XVME-540

Analog I/O Module

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Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The XVME-540 Analog Input/Output Module (also referred to as the AIO) is a powerful VMEbus compatible module, capable of performing both analog to digital and digital to analog conversions, with 12-bit resolution. The AIO can be configured to provide either 32 single-ended or 16 differential input channels, with 3 ranges of programmable gain, and 4 programmable input sampling modes. The module provides 4 output channels, with each channel configurable for either voltage or current-loop output operations. Power for the analog outputs is provided by an on-board DC/DC converter.

The XVME-540 AIO Module is designed around XYCOM's Standard I/O Architecture, which provides all XVME modules with standardization and compatibility in module addressing, in checking module identification and operational status, interrupt control, and module intercommunication.

1.2 MANUAL STRUCTURE

It is the aim of this first chapter to introduce the user to the general specifications and functional capabilities of the XVME-540 AIO Module. Successive chapters will develop the various aspects of module specification and operation in the following progression:

Chapter One - A general description of the Analog Input/Output Module, including complete functional and environmental specifications, VMEbus compliance information, and a detailed block diagram.

Chapter Two - Module installation information covering module specific system requirements, jumpers, and connector pinouts.

Chapter Three - Presents information required to program the AIO module for standard analog input and analog output operations.

Chapter Four - A short chapter covering the procedures for both input and output analog circuit calibration.

The appendices at the rear of this manual are designed to introduce and reinforce a variety of module-related topics including: XYCOM's Standard I/O Architecture, backplane signal/pin descriptions, a block diagram and schematics, and a quick reference section.

1.3 MODULE OPERATIONAL DESCRIPTION

Figure 1-1 shows an operational block diagram of the XVME-540 Analog Input/Output Module.

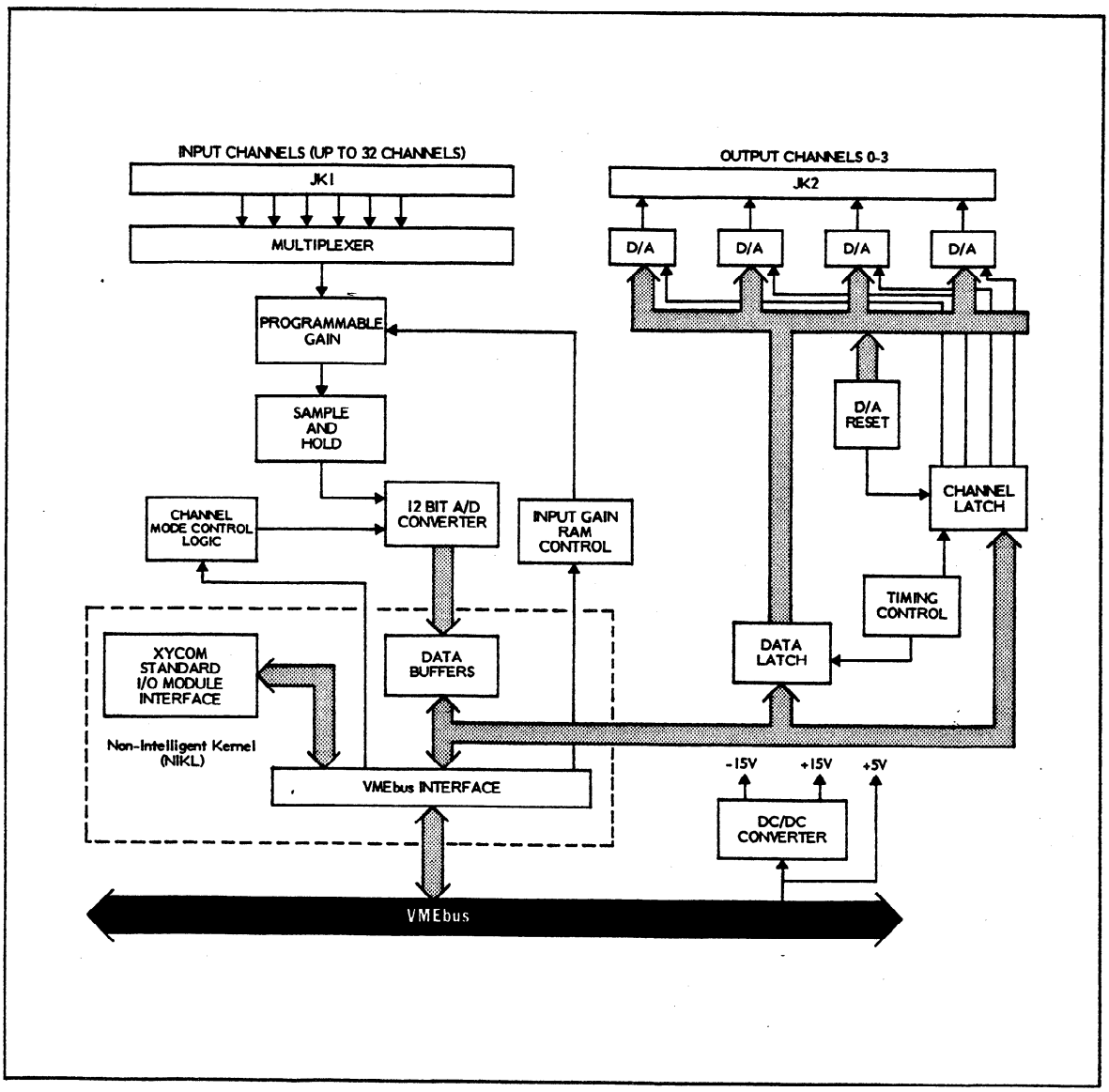


Figure 1-1. XVME-540 Operational Block Diagram

As can be seen from Figure 1-1, the AIO consists of the Non-Intelligent Kernel (NIKL) which is standard for XYCOM's non-intelligent VMEbus modules, and two application circuits, one to carry out analog to digital conversions and the other to carry out digital to analog conversions.

1.3.1 XYCOM Non-Intelligent Kernel

The Non-Intelligent Kernel is basically the interface to the VMEbus. It provides all of the necessary circuitry to receive and generate the signals required by the VMEbus specification for a 16-bit slave. By simply adding the application circuitry (in this case both D/A and A/D conversion circuitry), an XVME module is complete. The Non-Intelligent Kernel has the following features:

- Control and Address Buffers
- Address Decode circuitry
- Status/Control Register
- Module Identification information
- Module Self-Test capability with Pass/Fail LED indicators

The XYCOM Non-Intelligent Kernel is described in further detail in Appendix A.

1.3.2 Application Circuitry

As Figure 1-1 shows, the application circuitry consists of the following two parts:

Digital to Analog conversion circuitry -

- 4 D/A converters which perform 12-bit resolution D/A conversions.
- Data latch to store the digital data which is to be converted to an analog format.
- Channel latch to select the output channel over which the converted data will be output.
- Timing control to provide the proper timing sequence for 12-bit conversions.
- A reset feature which causes the digital to analog converters to be loaded with either all logic 1's or all logic 0's (jumper-selectable user option) at system power-up.

Analog to Digital conversion circuitry -

- A multiplexer which is directed by software to select one channel for data conversion.
- Programmable gain RAM allows the input gain for each channel to be programmed independently after power-up, over one of three ranges (with no need for constant reprogramming), to provide for increased conversion resolution on smaller input signals.

- Sample and Hold circuitry "samples" the input signal for approximately 24uS to allow for "settling time" in the Instrumentation Amplifier and Sampling circuitry. This signal is then "held" until the conversion is completed.

1.4 FEATURES OF XYCOM'S STANDARD I/O ARCHITECTURE

The AIO and all XYCOM XVME I/O modules conform to the XYCOM VMEbus Standard I/O Architecture. This architecture is intended to make the programming of XYCOM VMEbus I/O modules simple and consistent. The following features apply to the operation of the AIO Module.

- Module Address Space -- The AIO and all XVME modules are controlled by writing to addresses within the 64K Short I/O Address Space (or the VMEbus Standard Address Space). A module can be configured to occupy any of 64 available 1K blocks within the Address Space. The 1K block occupied by the module (known as the I/O Interface Block) contains all of the module's programming registers, module identification data, and I/O registers. Within the I/O Interface Block, the address offsets are standardized so that the user may expect to find the same registers and data at the same address offsets across the entire XYCOM XVME product line.

- Module Identification -- The AIO has I.D. information which provides the module name, model number, manufacturer and revision level at a location that is consistent with other XYCOM I/O modules.

- Status/Control Register -- This register is always located at address module base +81H, and the lower four bits (two Test Status bits, and a red and green LED bit) are standard from module to module.

A detailed description of XYCOM I/O Architecture is presented in Appendix A at the rear of this manual.

1.5 SPECIFICATIONS

Analog Input/Output Module Specifications

Characteristic	Specification
Analog Outputs	
Number of Channels	4
Accuracy	
Resolution	12 bits
Overall Error	±1/2 LSB
Differential Linearity	± 1 LSB
Voltage Output Characteristics	
Ranges	0-5V, 0-10V, ±5V, ±10V
Output Current	5mA min. @ ±10V
Settling Time	7 uS
Offset T.C.	75ppm/ °C
Gain T.C.	100ppm/ °C
Current Loop Characteristics	
Range	4-20mA, Non-isolated
Compliance Voltage	10V @ 20mA
Loop Supply Voltage	+15V to +30V
Settling Time	50 uS
Load Resistance Range	50 - 500 Ohms
Offset T.C.	75ppm/ °C
Gain I.C.	100ppm/ °C
Digital Input Coding	BIN, OBN
Analog Inputs	
Number of Channels	
Single-Ended	32
Differential	16
A/D Input Full Scale Voltage Ranges (Gain = 1)	
Unipolar	0-5V, 0-10V
Bipolar	±2.5V, ±5V, ±10V
Programmable Gain	
Range 1	1, 2, 5, or 10
Range 2	4, 8, 20, or 40
Range 3	10, 20, 50, or 100
Maximum Input Voltage	
Power On	44V
Power Off	30V

Analog Input/Output Module Specifications (continued)

Characteristic	Specification
Input Impedence	
With 22M ohm resistor	17M ohm min.
W/o 22M ohm resistor	100M ohm min.
Bias Current	±100nA
Input Capacitance	225 pF, max.
Operating Common Mode Voltage	14V
Accuracy	
Resolution	12 bits
Linearity	± 1/2 LSB
Differential Linearity	± 1/2 LSB
Monotonicity	Guaranteed
System Accuracy	
Gain = 1	±0.05% FSR, max.
Gain = 10	±0.1% FSR, max.
Gain = 100	±0.1% FSR, max.
System Accuracy Temp. Drift	
Gain = 1	40ppm/ °C, max.
Gain = 10	75ppm/ °C, max.
Gain = 100	110ppm/ °C, max.
Common Mode Rejection Ratio	60 db, min.
Speed	
Conversion Time	
Single Mode	25 uS
All other modes	50 uS
Throughput	
Single Mode	40KHz
All other modes	20KHz
External Trigger to Sample	25 uS
Environmental	
Temperature	
Operating	0 to 65 C
Non-operating	-40 to 85 C
Humidity	
Operating	5 to 95% RH non-condensing
Shock	
Operating	30g peak, 11mSec.
Non-operating	50g peak, 11mSec.

Analog Input/Output Module Specifications (continued)

Characteristic	Specification
Vibration	
Operating	.015 in. peak-to-peak 2.5g max.
Non-operating	.030 in. peak-to-peak 5.0g max.
Board Requirements	
Voltage	+5 VDC, ± 5%
Current	
Typical	2.75A
Maximum	3.00A
Board Dimensions	NEXP Board Size (160mm x 220mm)

VMEbus COMPLIANCE
• Fully compatible with VMEbus standard • A16:D16 DTB Slave • Any of I(1-7) Interrupter (STAT) • AM Codes 29, 2D, 39, 3D response (STAT)

Chapter 2

INSTALLATION

2.1 GENERAL

This chapter provides the information needed to configure and install the AIO Module.

2.2 SYSTEM REQUIREMENTS

The AIO Module is a double-height VMEbus compatible module. To operate it must be properly installed in a VMEbus backplane cardcage. The minimum system requirements for operation of the AIO Module are one of the following:

A) - A host processor installed on the same backplane.

- A properly installed controller subsystem. An example of such a controller subsystem is the XYCOM XVME-010 System Resource Module (SRM).

*** OR ***

B) - A host processor which incorporates an on-board controller subsystem.

2.3 LOCATION OF COMPONENTS RELEVANT TO INSTALLATION

The jumpers, address switches, interrupt level switches, calibration potentiometers, and connectors on the AIO Module are illustrated in Figure 2-1.

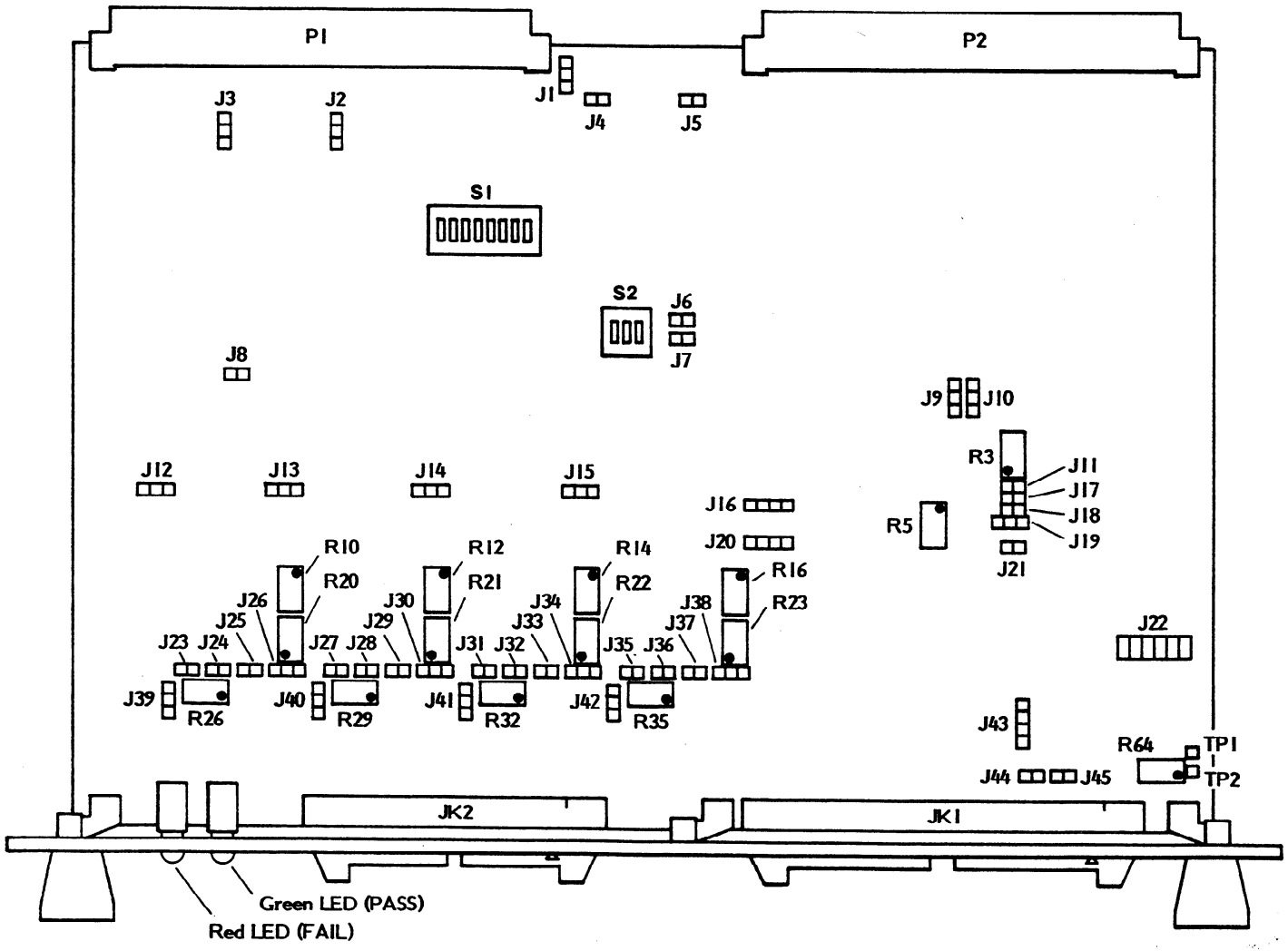


Figure 2-1. AIO Jumpers, Address Switches, Test Points, Calibration Potentiometers, and Connectors.

2.4 JUMPERS/SWITCHES

Prior to installing the AIO Module, it will be necessary to configure several jumper and switch options. The configuration of the jumpers and switches is dependent upon which of the variety of modes and module capabilities is required for the application. The jumper and switch options can be divided into three catagories: VMEbus-related options, analog to digital conversion options, and digital to analog conversion options.

VMEbus Options

Switch Bank S1	Use
Switches 1-6	Module base address select (refer to Section 2.5.1).
Switch 7	This switch determines whether the module will respond to only supervisory accesses or to both supervisory and non-privileged accesses (refer to Section 2.5.3).
Switch 8	This switch works in conjunction with jumper J2 to determine whether the board operates with address modifiers for the short I/O address space or those for the standard address space (refer to Section 2.5.2).
Switch Bank S2	**Use**
Switches 1-3	Interrupt level select for any interrupts generated by the module (refer to Section 2.5.5).
Jumpers	**Use**
J1	Selects either the use of on-board IACK* arbitration or the routing of the IACKIN* signal directly to the IACKOUT* signal, at the P1 connector. This jumper works in conjunction with jumper J3. If jumper J3 is not set to enable on-board IACK* arbitration, the daisy-chain will not be complete (refer to Section 2.5.6).
J2	This jumper works in conjunction with switch bank S1 (switch 8) for address space selection (i.e., short I/O address space or standard address space). (Refer to Section 2.5.2.)
J3	This jumper either enables or disables the on-board IACK* arbitration circuitry. The on-board arbitration must be enabled if the board is to be a part of IACK* daisy-chain (refer to Section 2.5.6).

Digital to Analog Conversion Options

Jumpers	Use
J8	This jumper will automatically set the D/A data lines to either all logic "1's" or all logic "0's" during system reset or power-up (refer to Section 2.6.1).
J12-J15	These jumpers provide the option to individually configure the output channels to convert either straight binary to analog or to convert two's complement binary to analog (refer to Section 2.6.2).
(J23,J24,J25,J26) (J27,J28,J29,J30) (J31,J32,J33,J34) (J35,J36,J37,J38)	These groups of jumpers select one of five output voltage ranges for each output channel. Four of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar voltage offset or for the adjustment of bipolar voltage offset (refer to Section 2.6.4).
J39-J42	These jumpers configure the four output channels to convert data to either an analog voltage format or an analog current format (refer to Section 2.6.3).

Analog to Digital Conversion Options

Jumpers	Use
J9 and J10	These jumpers provide the option of converting analog inputs to either a two's complement format or to a straight/offset binary format (refer to Section 2.7.1).
J16,J20, and J43	These jumpers are all used together to determine if the inputs will be configured as 16 differential or as 32 single-ended lines (refer to Section 2.7.2).
J17 and J21	These jumpers are used to configure the inputs for either bipolar or unipolar input voltages (refer to Section 2.7.3).
J18	This jumper configures the input voltage range for 0-5V and ±2.5V inputs (refer to Section 2.7.3).
J19	This jumper selects the 0-10V input range (refer to Section 2.7.3).
J22(cluster)	This jumper configuration selects one of three input stage gain ranges for the input channels (refer to Section 2.7.4).
J44 and J45	These two jumpers are provided to allow grounding of an input channel in either the single-ended or the differential input mode of operation for purposes of calibration (refer to Section 2.7.5).

2.5 VMEbus OPTIONS

2.5.1 Base Address Selection Switches (S1-1 to S1-6)

The XVME-540 AIO Module is designed to be addressed within either the VMEbus Short I/O or in Standard Memory Space. Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for XVME I/O modules has been designed to be switch (or jumper) selectable. When the XVME-540 Module is installed in the system, it will occupy a 1K byte block of Short I/O Memory or Standard Address Space. This 1K byte block is referred to as the I/O Interface Block.

The base address decoding scheme for XYCOM I/O modules is such that the starting address for each I/O Interface Block resides on a 1K boundary. Thus the module base address may be set to any one of 64 possible 1K boundaries within the Short I/O Address Space or any 1K boundaries with the Standard Address Space's upper 64K.

The module base address is selected by using the switches labeled 1-6 in DIP switch bank S1. Figure 2-2 shows the switch bank S1 and how the individual switches (1-6) relate to the base address bits.

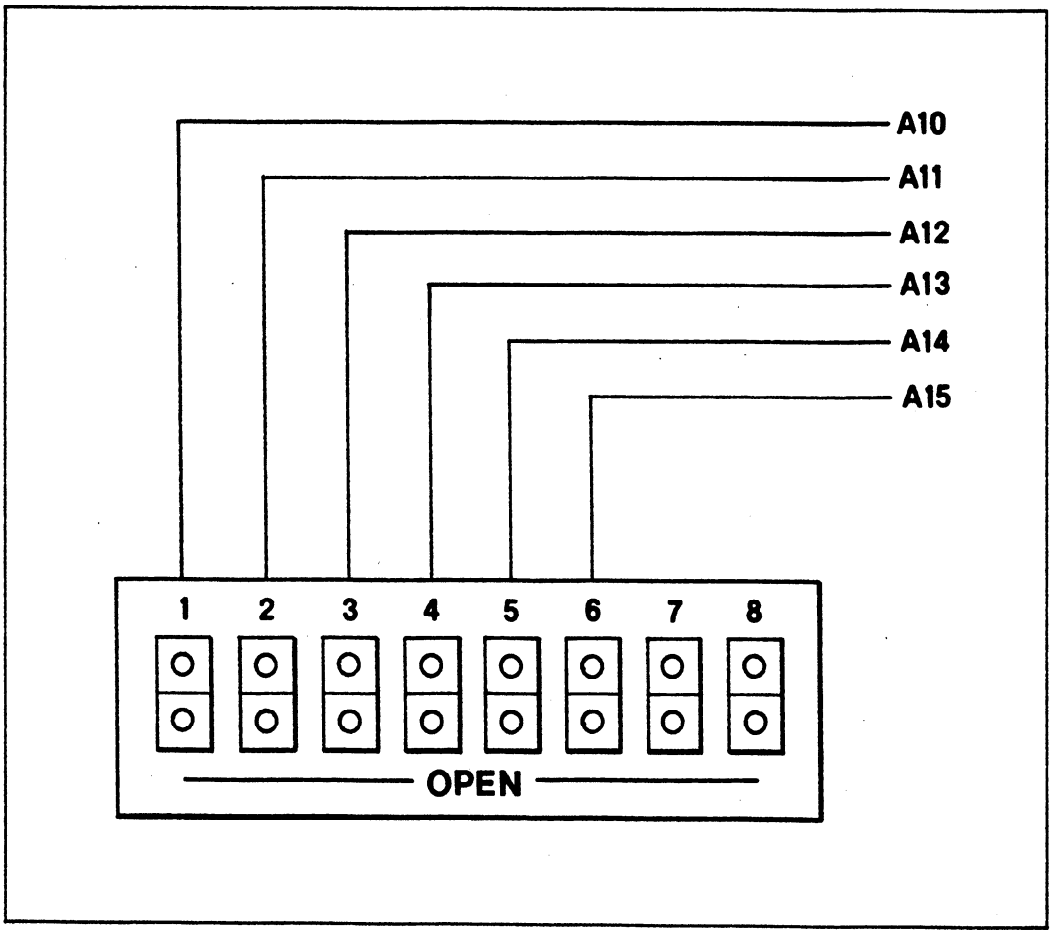


Figure 2-2. Switch Bank S1 - Base Address Switches

When a switch is in the closed position (i.e., when it is pushed in on the opposite end of the switch bank from the "open" label), the corresponding base address bit will be logic "0". When a switch is set to the open position, the corresponding base address bit will be logic "1".

Table 2-1 shows a list of the 64 1K boundaries which can be used as module base addresses in both the Short I/O Address Space and the Standard Memory Space, as well as the corresponding switch settings (switches 1-6) from S1.

Table 2-1. Base Address Switch Options

Switches						VME base address in VME Short I/O Address space
6(A15)	5(A14)	4(A13)	3(A12)	2(A11)	1(A10)	
0	0	0	0	0	0	0000H
0	0	0	0	0	1	0400H
0	0	0	0	1	0	0800H
0	0	0	0	1	1	0C00H
0	0	0	1	0	0	1000H
0	0	0	1	0	1	1400H
0	0	0	1	1	0	1800H
0	0	0	1	1	1	1C00H
0	0	1	0	0	0	2000H
0	0	1	0	0	1	2400H
0	0	1	0	1	0	2800H
0	0	1	0	1	1	2C00H
0	0	1	1	0	0	3000H
0	0	1	1	0	1	3400H
0	0	1	1	1	0	3800H
0	0	1	1	1	1	3C00H
0	1	0	0	0	0	4000H
0	1	0	0	0	1	4400H
0	1	0	0	1	0	4800H
0	1	0	0	1	1	4C00H
0	1	0	1	0	0	5000H
0	1	0	1	0	1	5400H
0	1	0	1	1	0	5800H
0	1	0	1	1	1	5C00H
0	1	1	0	0	0	6000H
0	1	1	0	0	1	6400H
0	1	1	0	1	0	6800H
0	1	1	0	1	1	6C00H
0	1	1	1	0	0	7000H
0	1	1	1	0	1	7400H
0	1	1	1	1	0	7800H
0	1	1	1	1	1	7C00H
1	0	0	0	0	0	8000H
1	0	0	0	0	1	8400H
1	0	0	0	1	0	8800H
1	0	0	0	1	1	8C00H
1	0	0	1	0	0	9000H
1	0	0	1	0	1	9400H
1	0	0	1	1	0	9800H
1	0	0	1	1	1	9C00H
1	0	1	0	0	0	A000H
1	0	1	0	0	1	A400H
1	0	1	0	1	0	A800H
1	0	1	0	1	1	AC00H
1	0	1	1	0	0	B000H
1	0	1	1	0	1	B400H
1	0	1	1	1	0	B800H
1	0	1	1	1	1	BC00H
1	1	0	0	0	0	C000H
1	1	0	0	0	1	C400H
1	1	0	0	1	0	C800H
1	1	0	0	1	1	CC00H
1	1	0	1	0	0	D000H
1	1	0	1	0	1	D400H
1	1	0	1	1	0	D800H
1	1	0	1	1	1	DC00H
1	1	1	0	0	0	E000H
1	1	1	0	0	1	E400H
1	1	1	0	1	0	E800H
1	1	1	0	1	1	EC00H
1	1	1	1	0	0	F000H
1	1	1	1	0	1	F400H
1	1	1	1	1	0	F800H
1	1	1	1	1	1	FC00H

NOTE Open = Logic "1"
Closed = Logic "0"

2.5.2 Address Space Selection (J2)

The user is given the option of placing the AIO Module in either VMEbus Short I/O or in Standard Memory Space. This selection is made by configuring jumper J2 and switch 8 of Switch Bank S1 (see Figure 2-2) as shown in Table 2-2 below.

Table 2-2. Addressing Options

Jumper	Switch 8 (S1)	Option Selected
J2A	Open	Standard Data Access Operation
J2B	Closed	Short I/O Access Operation

If jumper J2A is installed, Switch 8 (on switch bank S1) must be set to OPEN position.

If jumper J2B is installed, Switch 8 must be set to CLOSED position.

The XYCOM Standard I/O Architecture design specification recommends that the XVME-540 AIO Module operate within the Short I/O Address Space, in order to take advantage of the Standard I/O Architecture's various features (refer to Appendix A for a description of features).

If required, the AIO Module can operate in the Standard Address Space. The user should note that in this mode, due to the address decoding scheme, the AIO Module will always reside within the upper 64K byte segment of the Standard Memory Address Space (i.e., the address range FF0000H through FFFFFFH). Switches 1 through 6 of the Switch Bank S1 then determine which 1K block of the upper 64K byte segment is to be occupied.

2.5.3 Supervisor/Non-Privileged Mode Selection

The AIO Module can be configured to respond to only Supervisory access, or to both Non-Privileged and Supervisory accesses, by selecting the position of Switch 7 (located in Switch Bank S1, see Figure 2-2), as shown in Table 2-3.

Table 2-3. Privilege Options

Switch S7 (of bank S1)	Privilege Mode Selected
Closed	Supervisory or Non-Privileged
Open	Supervisory Only

2.5.4 Address Modifier Reference

The following table (Table 2-4) indicates the actual VMEbus Address Modifier code that the AIO Module will respond to, based on the status of the two options discussed in the previous two sections.

Table 2-4. Address Modifier Code Options

Address Space	Switches (of S1) 7	8	Jumper J2	Address Modifier Code AIO Module will respond to
Normal	Closed	Closed	B	29H or 2DH
Short I/O	Open	Closed	B	2DH only
Standard	Closed	Open	A	39H or 3DH
Address	Open	Open	A	3DH only

2.5.5 Interrupt Level Switches (S2)

The three Interrupt Level Switches select which VMEbus interrupt level is to be used by the module. The AIO Module can be programmed to generate an interrupt at the completion of a conversion, and these switches will determine the level of that interrupt. The interrupt level switch options are defined in Table 2-5.

Table 2-5. Interrupt Level Switches (S2)

S2-3	S2-2	S2-1	VMEbus Interrupt Level
Open	Open	Open	7
Open	Open	Closed	6
Open	Closed	Open	5
Open	Closed	Closed	4
Closed	Open	Open	3
Closed	Open	Closed	2
Closed	Closed	Open	1
Closed	Closed	Closed	None, interrupts disabled

2.5.6 Interrupt Acknowledge (IACK*) Enable Jumpers (J1,J3)

When operating in an interrupt environment, the AIO Module uses the VMEbus IACK* daisy-chain to determine which module gets acknowledged in cases where two or more modules share one of the interrupt request lines. When the module is not going to be used in an interrupt environment, the daisy-chain through the module can be bypassed to speed up the IACK* arbitration. This is controlled by jumpers J1 and J3, where J1 connects/disconnects IACKIN* to the module and J2 engages/disengages the on-board arbitration circuitry. Table 2-6 shows the Interrupt Acknowledge options.

Table 2-6. IACK* Enable Jumpers

Jumper Settings J1	Jumper Settings J3	Option
Position A	Position A	Module bypasses IACK* daisy chain
Position B	Position B	Module uses IACK* daisy chain

With the jumpers in the "A" position, the module cannot respond to interrupts because IACKIN* is not monitored and the on-board arbitration is not engaged. In the "A" position the module directly connects IACKIN* to IACKOUT*.

When interrupts are going to be used, the jumpers must be in the "B" position.

2.6 DIGITAL to ANALOG CONVERSION OPTIONS

2.6.1 Analog Output Reset Jumper (J8)

Depending on how J8 is configured, the four digital to analog converters will be loaded with either logic "1's" or logic "0's" at reset or power-up. Table 2-7 shows the two configuration possibilities.

Table 2-7. Analog Output Reset Jumper (J8)

Jumper	Digital State Converted to Analog on All Outputs
Out	Logic 1
In	Logic 0

NOTE

This reset capability only applies to the outputs after a system (backplane) reset, or at power-up. It does not occur after a software reset is issued to the module. (Refer to Chapter 3 for information on software reset.)

2.6.2 Output Conversion Format Jumpers (J12-J15)

This jumper option provides a means of configuring the D/A conversion circuitry to handle digital data in either the straight/offset binary formats, or in the two's complement binary format. The use of this option is entirely dependent upon the data format which is provided by the output control program being employed by the user. Each of the four output channels can be configured independently, as shown in Table 2-8.

Table 2-8. Output Conversion Format Jumpers

Output Channel	Digital Data Conversion Formats	
	Straight/Offset Binary	Two's Complement Binary
3	J12A	J12B
2	J13A	J13B
1	J14A	J14B
0	J15A	J15B

2.6.3 **Voltage/Current Output Selection Jumpers**

Each of the four analog output channels is capable of providing an output which can be used as a voltage applied source, or as a current applied source. Prior to configuring any other channel specific criteria, it should be determined whether the output will be used as an analog voltage source or as an analog current source. Table 2-9 shows which jumpers configure the channels for outputs based on current, and which jumpers configure the channels for outputs based on voltage.

Table 2-9. Voltage/Current Output Selection Jumpers

Output Channel	Output	
	Current	Voltage
0	J42B	J42A
1	J41B	J41A
2	J40B	J40A
3	J39B	J39A

When a channel is to be configured for voltage output, a corresponding voltage range must be selected and jumpered (refer to Section 2.6.4). Depending on whether the voltage range selected is unipolar or bipolar, a channel specific potentiometer is jumper selected (refer to Section 2.6.4), and offset voltage calibration can be performed (refer to Chapter 4 for calibration information).

When a channel is configured for current output, the voltage range selection jumpers which correspond to that particular channel must be configured for the 0-10V range (see note in Section 2.6.4). The specified current loop range for each output channel is 4-20mA.

2.6.4 **Output Voltage Range Selection Jumpers (J23-J38)**

All four output channels can be jumper configured to provide analog output voltages in any one of five voltage ranges. There are three bipolar output voltage ranges and two unipolar output voltage ranges. The bipolar ranges are:

±2.5V
±5V
±10V

The unipolar ranges are:

0 to +5V
0 to +10V

Each output channel has its own group of three jumpers which determine which of the five output voltage ranges will apply to that channel. In addition, each output channel has a corresponding jumper which activates an offset voltage calibration potentiometer, and thus allows offset adjustment for either bipolar or unipolar operation. Table 2-10 shows the various jumper combinations used to configure the output channels for the specific voltage ranges. Note that the last jumper in each group (i.e., J26, J30, J34, J38) is the jumper which activates the offset voltage calibration potentiometer for either unipolar or bipolar adjustment on each channel (refer to Chapter 4 for calibration procedure).

Table 2-10. Output Voltage Range Configurations

Channel	Jumper	Output Voltage Ranges				
		±2.5V	±5V	±10V	0-5V	0-10V
3	J23	Out	In	In	Out	In
3	J24	In	In	Out	In	In
3	J25	In	Out	Out	In	Out
3	J26	A	A	A	B	B
2	J27	Out	In	In	Out	In
2	J28	In	In	Out	In	In
2	J29	In	Out	Out	In	Out
2	J30	A	A	A	B	B
1	J31	Out	In	In	Out	In
1	J32	In	In	Out	In	In
1	J33	In	Out	Out	In	Out
1	J34	A	A	A	B	B
0	J35	Out	In	In	Out	In
0	J36	In	In	Out	In	In
0	J37	In	Out	Out	In	Out
0	J38	A	A	A	B	B

NOTE

When using a channel in the current output mode (refer to Section 2.6.3), the voltage output jumpers for that channel must be configured for the 0-10V range.

2.7 ANALOG to DIGITAL CONVERSION OPTIONS

2.7.1 Input Conversion Format Jumpers (J9 and J10)

This jumper option provides a means of configuring the A/D conversion circuitry to convert analog information to either the straight/offset binary formats, or to the two's compliment binary format. The use of this option will be entirely dependent upon the data format which is required by the input control program being employed by the user. This option is inclusive to all input channels and cannot be utilized on an individual channel basis. Table 2-11 shows the jumper options.

Table 2-11. Input Conversion Format Jumpers

Jumpers	Digital Data Conversion Format Jumpers
J9B and J10B*	Analog to straight binary or offset binary
J9A and J10A*	Analog to two's complement binary

* These jumpers must be inserted together (i.e., J9B and J10B, and J9A and J10A) in order for this option to work properly.

2.7.2 Differential/Single-Ended Input Option Jumpers

The analog input portion of the AIO Module can be configured to provide either 32 single-ended or 16 differential input channels. The two modes are mutually exclusive so that the module will accept either all single-ended inputs or all differential inputs, but not a combination of both. Selection of single-ended vs. differential mode is done via jumpers J16, J20, and J43. Table 2-12 shows the jumper options.

Table 2-12. Single-Ended vs. Differential Input Selection

Jumpers Set	Input Mode
J16A,J16C J20A,J20C J43A,J43C	When these six jumpers are set in this manner, the module inputs will be configured for single-ended operation.
J16B J20B J43B	When these three jumpers are set in this manner, the module inputs will be configured for differential operation.

NOTE

Only one of the two jumper configurations may be installed at any one time. Make certain that if the board is to be used in the single-ended input mode, the jumpers for differential operation are removed; and likewise, if the board is to be used in the differential mode, the single-ended option jumpers should be removed.

The physical configuration of the input connector (JK1) will appear differently, depending on whether the module is jumpered for single-ended or differential input operation. Table 2-17 in Section 2.8 shows the pinout for connector JK1 and how the input connections appear for each of the two modes.

2.7.3 Input Voltage Type and Voltage Range Selection (J17, J18, J19, and J21)

The analog inputs may be configured to accept either bipolar or unipolar input voltages. Jumpers J17 and J21 determine which voltage type the module will accept. The analog input channels can be jumper-configured to accept voltages in any one of five ranges. There are three bipolar voltage ranges and two unipolar ranges.

Bipolar Ranges	Unipolar Range
±2.5V	0-5V
±5V	0-10V
±10V	

The ±2.5V (bipolar) range and the 0-5V (unipolar) range are selected by jumper J18. The ±10V (bipolar) range is selected by jumper J19. Table 2-13 shows the options.

Table 2-13. Voltage Type and Voltage Range Selection Options

Input Range	Install	Remove
Unipolar:		
0-5V	J21,J18	J17,J19
0-10V	J21,J19B	J17,J18
Bipolar:		
±2.5V	J17,J18	J21,J19
±5.0V	J17,J19B	J21,J18
±10.0V	J17,J19A	J21,J18

2.7.4 Input Gain Range Selection (J22 - Jumper Cluster)

The gain for each analog input channel is individually programmable over any one of three possible gain ranges. First the required range is selected by configuring jumper J22. Next, the specific gains (within the selected range) are determined by the user and written to on-board RAM during an input initialization procedure (refer to Section 3.3.4). Thereafter, any time an input is converted (A/D), it will automatically apply the gain factor for which it was previously programmed. The three input gain ranges are:

Range 1 -- 1, 2, 5, or 10

Range 2 -- 4, 8, 20, or 40

Range 3 -- 10, 20, 50, or 100

The various input gain ranges are selected by installing two jumpers for each option. The options and their corresponding jumpers are shown in Table 2-14.

Table 2-14. Input Gain Range Selection Jumpers

Jumpers Installed	Gain Range Selected
J22A and J22B	Range 1 (X1)
J22C and J22D	Range 2 (X4)
J22E and J22F	Range 3 (X10)

Only one range can be selected at a time, and the input channels can only be programmed for specific gains within the selected range.

2.7.5 Input Calibration Grounding Jumpers (J44 and J45)

These two jumpers are used to ground a single input channel in either the single-ended or the differential mode for purposes of programmable gain offset adjustment. If the inputs are configured for single-ended operation, inserting jumper J44 shorts input channel 8 to ground, and inserting J45 shorts channel 0 to ground. In differential mode, inserting both J44 (channel 0 Hi) and J45 (channel 0 Lo) will short channel 0 to ground. Table 2-15 shows the relationship between the jumpers and the grounded channels. Refer to Chapter 4 - Calibration, for exact input calibration procedure.

Table 2-15. Input Calibration Grounding Jumpers

Jumpers	Input Configuration	Channel Shorted to Ground
J44	Single-ended	Channel 8
J45	Single-ended	Channel 0
J44 & J45	Differential	Channel 0

2.8 EXTERNAL CONNECTORS JK1 and JK2

The analog input and output channels are accessible on the front panel of the board in the form of two mass termination headers (JK1 and JK2). Connector JK1 is a 50 pin header which contains all of the analog input connections. Connector JK2 is a 34 pin header which contains all of the analog output connections. Figure 2-3 shows the module front panel and the arrangement of connectors JK1 and JK2.

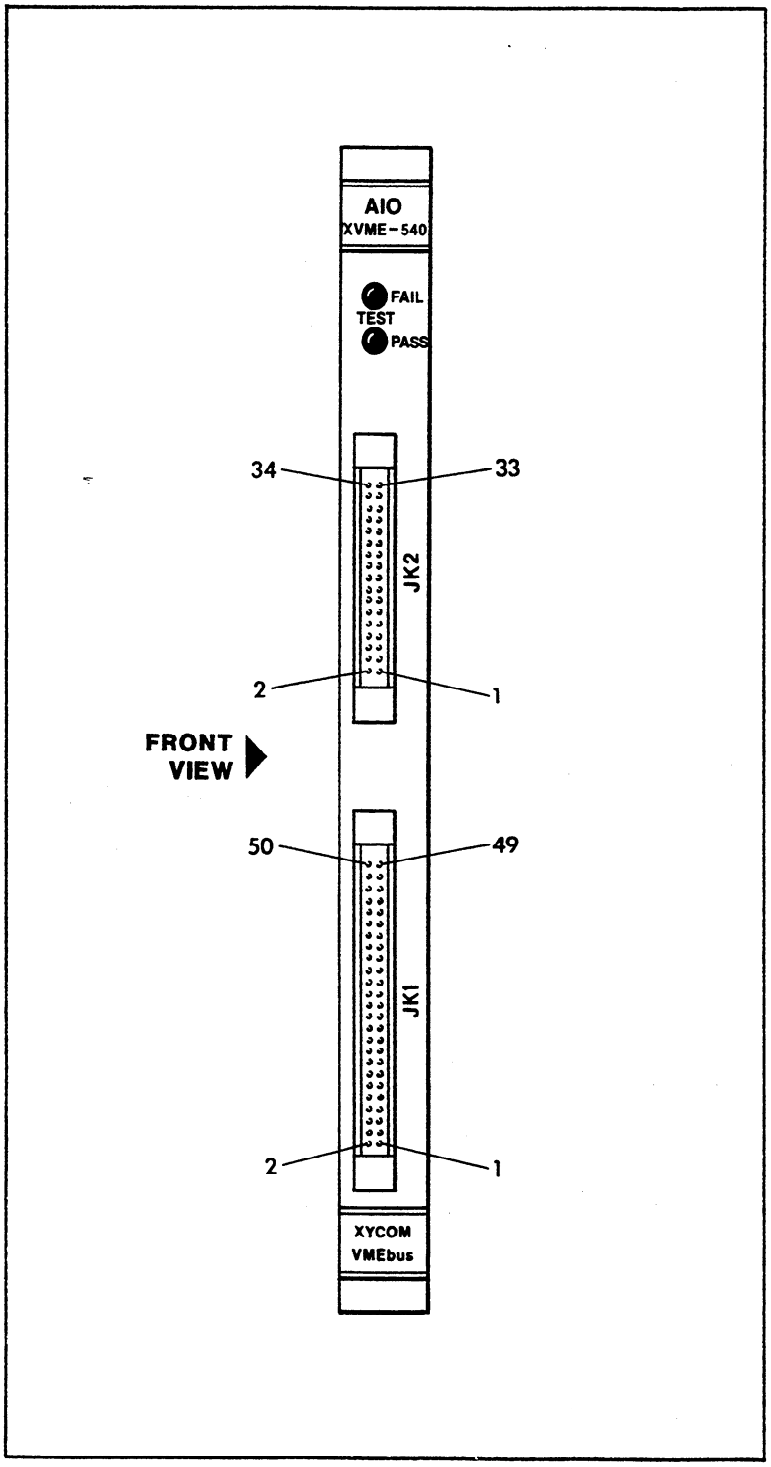


Figure 2-3. Connectors JK1 and JK2

NOTE

Pins 1 through 48 of Connector JK1 are fully compatible with Analog Devices 3B Series Universal Signal Conditioning System (Pins 49 and 50 are used for external trigger only). Pins 1-24 of Connector JK2 are compatible with Analog Devices 3B Series Universal Signal Conditioning System.

Table 2-16 shows the pin designation for connector JK1 and Table 2-17 shows the pin designations for connector JK2.

Table 2-16. Input Connector JK1

JK1

Pin	Single-ended Configuration	Differential Configuration
1	Channel 0	Channel 0 Lo
2	Channel 8	Channel 0 Hi
3	Analog Ground	Analog Ground
4	Channel 9	Channel 1 Hi
5	Channel 1	Channel 1 Lo
6	Analog Ground	Analog Ground
7	Channel 2	Channel 2 Lo
8	Channel 10	Channel 2 Hi
9	Analog Ground	Analog Ground
10	Channel 11	Channel 3 Hi
11	Channel 3	Channel 3 Lo
12	Analog Ground	Analog Ground
13	Channel 4	Channel 4 Lo
14	Channel 12	Channel 4 Hi
15	Analog Ground	Analog Ground
16	Channel 13	Channel 5 Hi
17	Channel 5	Channel 5 Lo
18	Analog Ground	Analog Ground
19	Channel 6	Channel 6 Lo
20	Channel 14	Channel 6 Hi
21	Analog Ground	Analog Ground
22	Channel 15	Channel 7 Hi
23	Channel 7	Channel 7 Lo
24	Analog Ground	Analog Ground
25	Channel 16	Channel 8 Lo
26	Channel 24	Channel 8 Hi
27	Analog Ground	Analog Ground
28	Channel 25	Channel 9 Hi
29	Channel 17	Channel 9 Lo
30	Analog Ground	Analog Ground
31	Channel 18	Channel 10 Lo
32	Channel 26	Channel 10 Hi
33	Analog Ground	Analog Ground
34	Channel 27	Channel 11 Hi
35	Channel 19	Channel 11 Lo
36	Analog Ground	Analog Ground
37	Channel 20	Channel 12 Lo
38	Channel 28	Channel 12 Hi
39	Analog Ground	Analog Ground
40	Channel 29	Channel 13 Hi
41	Channel 21	Channel 13 Lo
42	Analog Ground	Analog Ground
43	Channel 22	Channel 14 Lo
44	Channel 30	Channel 14 Hi
45	Analog Ground	Analog Ground
46	Channel 31	Channel 15 Hi
47	Channel 23	Channel 15 Lo
48	Analog Ground	Analog Ground
49	Power Ground	Power Ground
50	External Trigger	External Trigger

Table 2-17. Input Connector JK2

JK2

Pin	Description
1	Channel 0 Vout
2	NC
3	Analog Ground
4	NC
5	Channel 1 Vout
6	Analog Ground
7	Channel 2 Vout
8	NC
9	Analog Ground
10	NC
11	Channel 3 Vout
12	Analog Ground
13	NC
14	NC
15	Analog Ground
16	NC
17	NC

Pin	Description
18	Analog Ground
19	NC
20	NC
21	Analog Ground
22	NC
23	NC
24	Analog Ground
25	NC
26	NC
27	Channel 0 Iout+
28	Iout-
29	Iout-
30	Channel 1 Iout+
31	Channel 2 Iout+
32	Iout-
33	Iout-
34	Channel 3 Iout+

2.9 MODULE INSTALLATION

The XYCOM VMEbus modules can accommodate typical VMEbus backplane construction. Figure 2-4 shows a standard VME chassis and a typical backplane configuration. There are two rows of backplane connectors depicted (i.e., the P1 backplane and the P2 backplane).

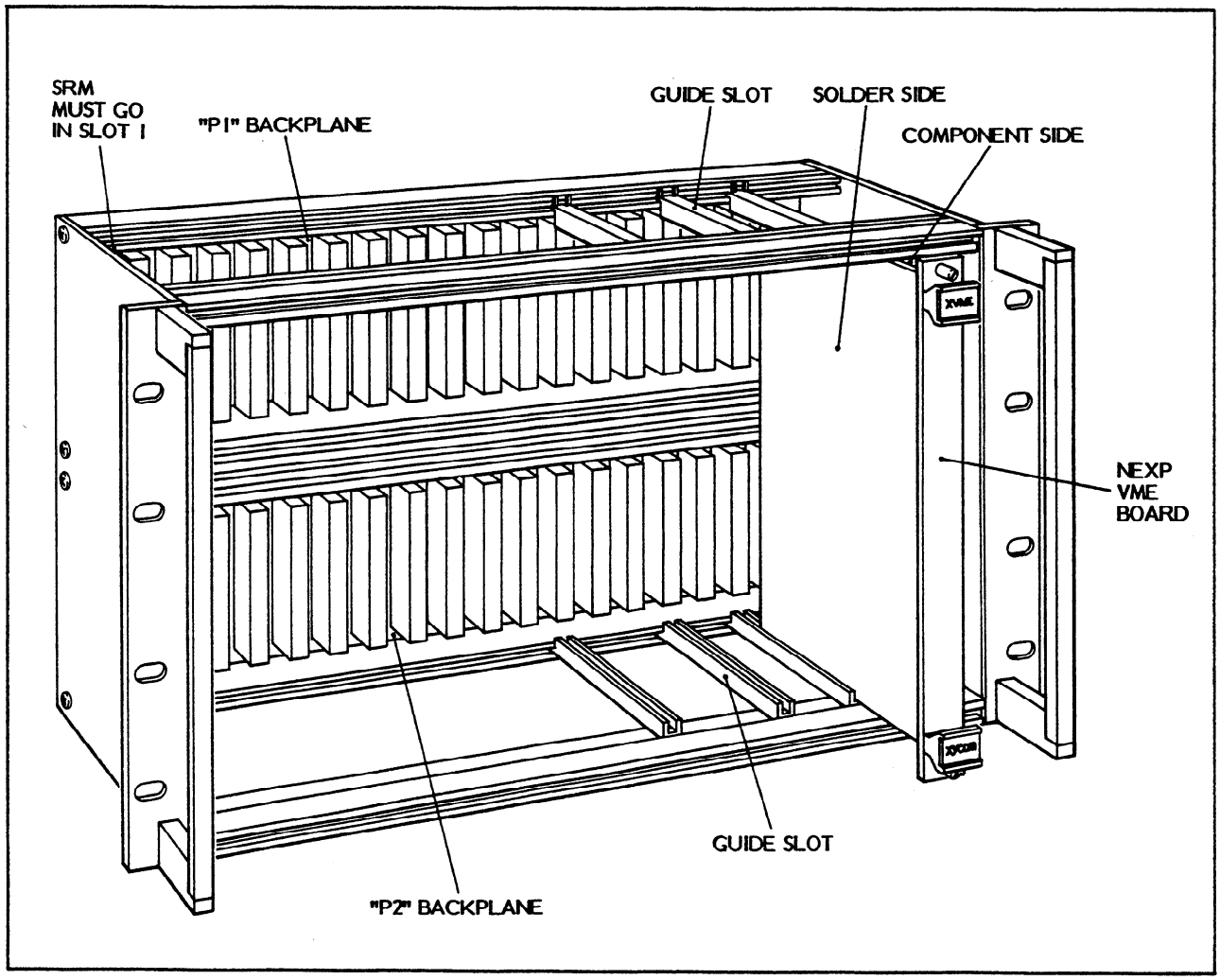


Figure 2-4. VMEbus Chassis

2.9.1 Installation Procedure

CAUTION

Do not attempt to install or remove any boards without first turning off the power to the bus and all related external power supplies.

Prior to installing a module, determine and verify all relevant jumper configurations and all connections to external devices or power supplies. (Please check the jumper configuration with the diagram and lists in the manual.)

To install a board in the cardcage, perform the following steps:

1) Make certain that the particular cardcage slot which you are going to use is clear and accessible.

2) Center the board on the plastic guides so that the solder side is facing to the left and the component side is facing to the right (refer to Figure 2-5).

3) Push the card slowly toward the rear of the chassis until the connectors engage (the board should slide freely in the plastic guides).

4) Apply straight-forward pressure to the two handles on the outer edge of the board until the connectors are fully engaged and properly seated.

NOTE

It should not be necessary to use excess pressure or force to engage the connectors. If the board does not properly connect with the backplane, remove the module and inspect all connectors and guide-slots for possible damage or obstructions.

5) Once the board is properly seated, it should be secured by tightening the two machine screws at the extreme top and bottom of the board.

Chapter 3

PROGRAMMING THE AIO MODULE

3.1 INTRODUCTION

This chapter provides the information required to program the AIO module for analog input and output signal conversions. This information is presented in the following fashion:

- Presentation of module address map showing programming locations
- A discussion of base addressing and the module I/O interface block
- A/D conversion modes
- D/A conversion principles

3.2 BASE ADDRESSING

The AIO module is designed to be addressed within either the VMEbus-defined 64K short I/O address space, or the upper 64K of standard address space. Since each I/O module connected to the bus must have its own unique base address, the base-addressing scheme for XYCOM XVME I/O modules has been designed to be switch-selectable. When the AIO module is installed in the system it will occupy a 1K byte block of address space (this 1K block is referred to as the I/O Interface Block). The base address decoding scheme for XVME I/O modules is such that the starting address for each I/O Interface Block resides on a 1K boundary. Thus, the module base address will be one of the 64 - 1K boundaries available within either the short I/O address space or the upper 64K of standard address space (refer to Chapter 2, Table 2-1 for a complete list of the 64 - 1K boundaries).

Figure 3-1 shows the I/O Interface Block for the AIO module.

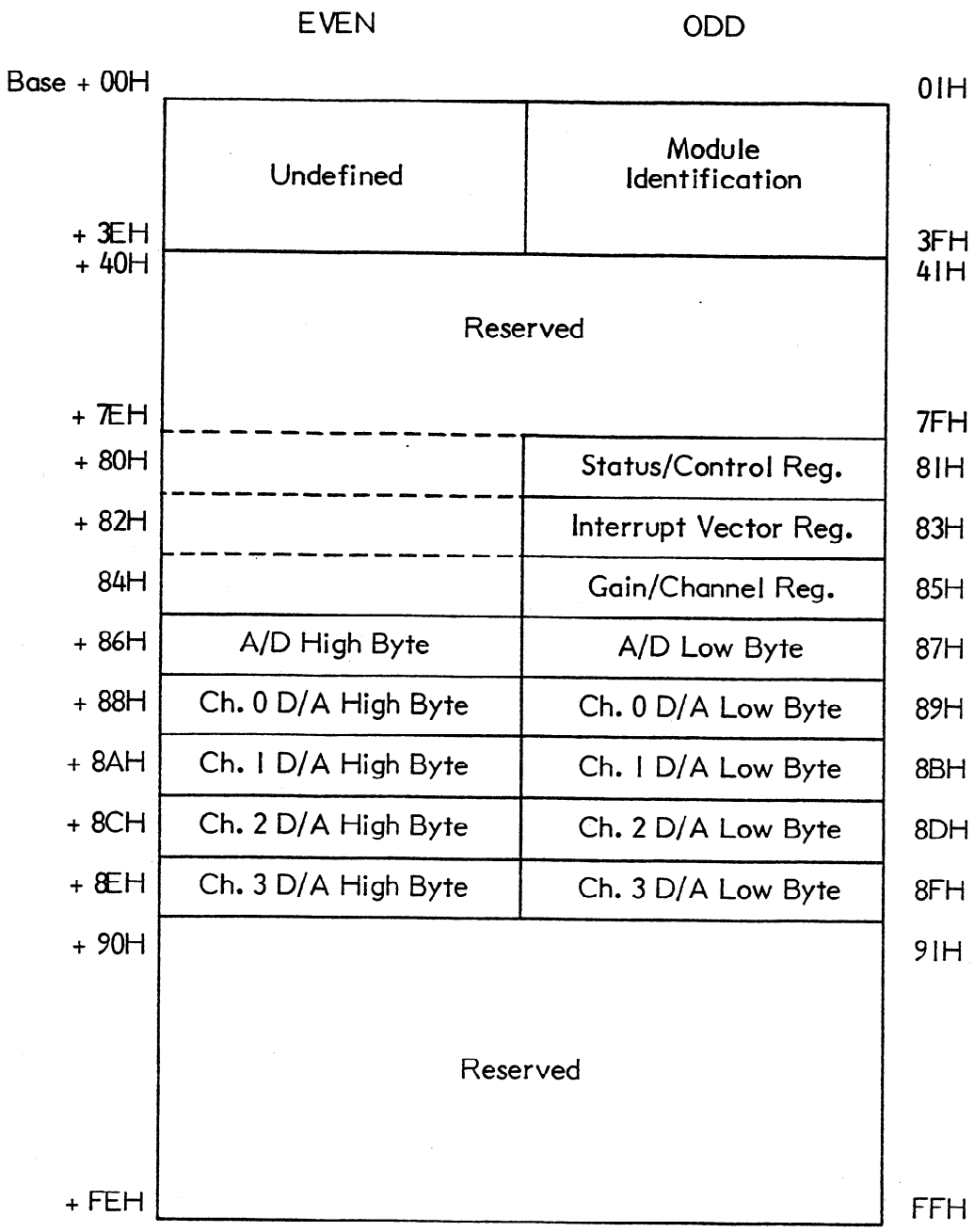


Figure 3-1. The AIO Module I/O Interface Block and the Short I/O Address Space.

Any location within the AIO module's 1K I/O Interface Block can be accessed by adding the module base address to the address of the specific location within the I/O Interface Block (referred to as the I/O Interface Block offset). For example, the module Status/Control Register is located at address 81H within the I/O Interface Block. If the module base address is set at 1000H then the Status/Control register would be accessible at address 1081H.

(Module base Address)		(I/O Interface Block Offset)		(Status/Control) Register)
1000H	+	081H	=	1081H

For memory-mapped CPU modules (such as 68000 CPU modules), the short I/O address space is memory-mapped to begin at a specific address. For such modules, the I/O Interface Block Offset is an offset from the start of this memory-mapped short I/O address space. For example, if the short I/O address space of a 68000 CPU module starts at F90000H and if the base address of the AIO is set at 1000H, the actual module base address would be F91000H.

3.3 I/O INTERFACE BLOCK

The I/O Interface Block of the AIO Module contains the following programming locations (as shown in Figure 3-1) which are defined in greater detail in their own sections of this chapter.

- Module I.D. information (base + 01H to base + 3FH): These locations provide information specifying model number, manufacturer, and revision level.

- Status/Control Register (base + 81H): The Status/Control Register contains eight single bit locations which provide control signals to turn on PASS and FAIL LEDs, reset the module, enable interrupts, start conversion, show if there are interrupts pending, and select the mode of analog input operation (i.e., single channel, sequential channel, random channel, and external trigger).

- Interrupt Acknowledge (IACK) Vector Register (base + 83H), which holds the vector to be driven onto the VMEbus when an interrupt generated by the AIO module is acknowledged.

- Gain/Channel Register (base + 85H): This register is used to initiate random channel conversions, and to program a 32 element input gain RAM as part of an input initialization procedure. The lower five bits of this register are used to select one of the input channels for conversion, or gain programming. The sixth bit determines whether the register is used to program gain, or to read the gain and convert a specific channel. The upper two bits are used to select one of four allowable gain settings to be programmed for a selected channel.

- A/D Input High Byte (base + 86H) and Low Byte (base + 87H): These locations contain the digital data which results from A/D (analog input) conversions.

- D/A Output High Byte (Chan.0 - Chan.3, base + 88H - 90H, even locations) and D/A Output Low Byte (Chan.0 - Chan.3, base + 89H - 91H, odd locations): The digital data written to these locations will be converted to analog. Conversion is automatically triggered by writing to the D/A Output Low Byte.

NOTE

Reading from or writing to undefined I/O Interface Block locations may make application software incompatible with future XVME modules.

3.3.1 **Module Identification Data**

The XYCOM module identification scheme provides a unique method of registering module-specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K byte blocks occupied by the module, and module functional revision level. This information can be read by the system processor on power-up to verify the system configuration and operational status. Table 3-1 defines the identification information locations.

Table 3-1. Identification Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier,
5	E	45	always "VMEID"
7	I	49	(5 characters)
9	D	44	
B	X	58	Manufacturer's I.D.,
D	Y	59	always "XYC" for XYCOM
F	C	43	modules (3 characters)
11	5	35	
13	4	34	Module Model Number
15	0	30	(3 characters and
17		20	4 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision
23	1	31	level with leading blank (if single digit)
25	1	30	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer
37	"		Dependent Information,
39	"		Reserved for future use
3B	"		
3D	"		
3F	"		

The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1H-3FH).

Thus, I.D. information can be accessed by addressing the module base, offset by the specific address for the character(s) needed. For example if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O Interface Block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex encoded ASCII value at each location. Thus, in this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH.

3.3.2 Status/Control Register (base + 81H)

Writing to the Status/Control Register can: control the red (FAIL) and green (PASS) LEDs, initiate an A/D conversion, select an A/D conversion mode, reset the module, and enable module interrupts to the VMEbus.

Reading from the Status/Control Register can indicate: whether or not a conversion is in progress or when a conversion is complete, if there are interrupts pending, and the status of the PASS/FAIL LEDs. Figure 3-2 defines the Status/Control bits.

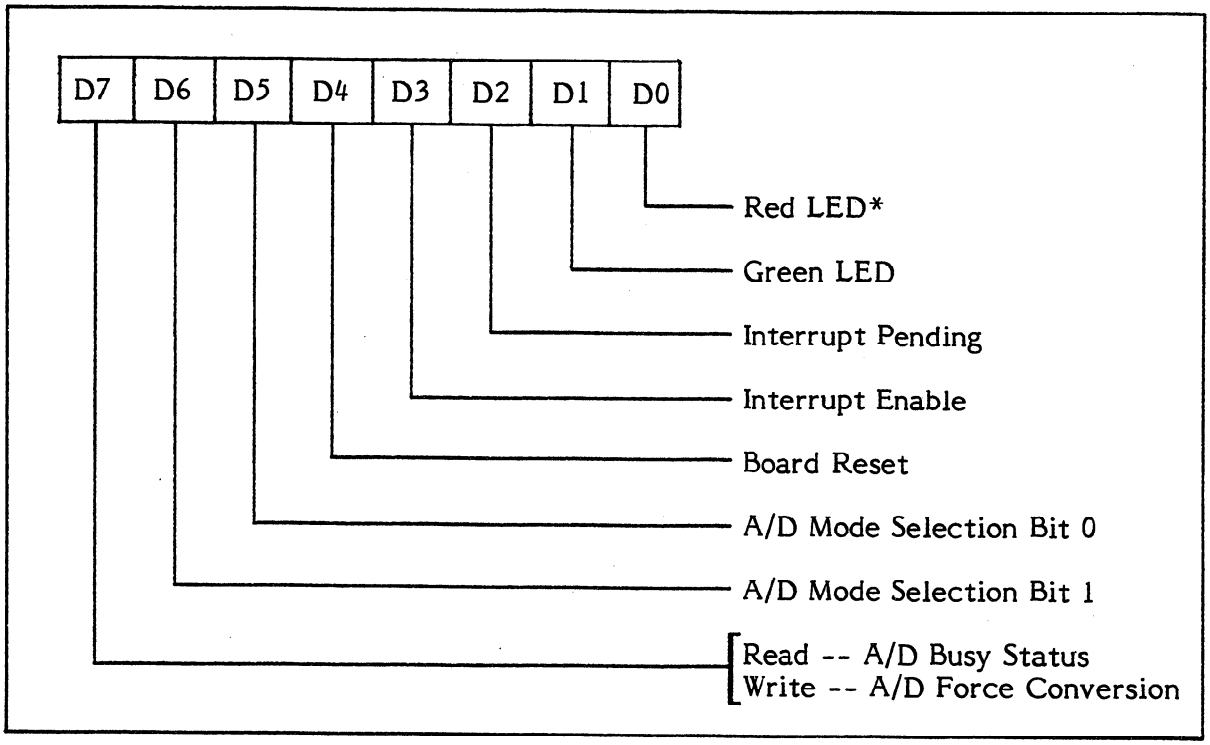


Figure 3-2. Status/Control Register

3.3.2.1 Status/Control Register Bit Definitions

D7: This bit acts as a "Busy" flag to show when an A/D conversion is in progress. A logic "1" at this location indicates that the analog input portion of the module is in the process of making an A/D conversion. The level of this bit should be checked prior to starting a new A/D conversion, or the conversion in progress could become corrupted. In addition, by writing a logic "1" to this bit, a conversion can be "force" started. This method of forcing a conversion works in any of the four A/D data conversion modes, and the length of the conversion is dependent upon which of the four A/D modes the board is operating in (i.e. 25uS for Single-Channel mode and 50uS for the other three modes).

D5&6: These two bits determine which of four analog input modes the module will operate in. Table 3-2 shows the four input mode options.

Table 3-2 Input Mode Options

Mode Bits		A/D Conversion Mode
Bit 6	Bit 5	
0	0	Single Channel
0	1	Sequential Channel
1	0	Random Channel
1	1	External Trigger

The use of the input conversion modes is explained in greater detail in Section 3.4.1.

D4: This bit provides a means for a module software reset. If this bit is "toggled" to logic "1" and back to logic "0", a software reset will occur. This action causes the "busy" flag (bit D7), the interrupt pending bit (bit D2), and the input latch used by the external trigger to reset.

D3: Assuming that the associated jumpers and switches are set appropriately, a logic "1" written to this location will enable the module to generate VMEbus interrupts.

D2: This bit is an interrupt pending flag. A logic "1" at this location indicates that an A/D conversion has been completed. The interrupt pending bit can be cleared in one of three ways:

1) By causing a new A/D conversion (see Bit D7).
2) By performing a backplane or a software reset (see Bit D4).
3) By reading the converted input data from the low order data byte.

D1&0: These bits control the red and green LEDs. The red and green LEDs provide a visual indication of the module status.

- A logic "0" at bit D0 turns on the Red LED
- A logic "1" at bit D1 turns on the Green LED

The LEDs should be used to indicate the following status (Table 3-1) as set forth by the XYCOM XVME Standard Architecture Design (also described in Appendix A). The AIO module is classified as a non-intelligent module, and thus all diagnostics for it must be performed by the system host.

Table 3-3. LED Status

Status Bits		LEDs		SYSFAIL*	Status
1	0	Green	Red		
0	0	Off	On	On	Module failed, or not yet tested
0	1	Off	Off	Off	Inactive module
1	0	On	On	On	Module undergoing test
1	1	On	Off	Off	Module passed test

NOTE

Whenever Bit 0 is at logic "0", the VMEbus signal SYSFAIL* will be asserted, and the Red LED will be on. The power-up or reset state for status bits is "00".

3.3.3 Interrupt Acknowledge (IACK) Vector Register (base + 83H)

The AIO Module is capable of generating an interrupt at the completion of an A/D conversion on any one of the seven levels allowed by the VMEbus specification. As was previously mentioned (Chapter 2, Section 2.4), the interrupt-level select switches, and the IACK daisy-chain enable jumpers are configured at the time of module installation. Interrupts are enabled, for example, by writing a logic "1" to bit D3 of the Status/Control Register (refer to Section 3.3.2.1). The Interrupt Acknowledge Vector Register is a write-only register that holds the vector to be driven on the VMEbus when the interrupt generated by the AIO module is acknowledged. The Interrupt Acknowledge Vector Register is accessible at the module base address + 83H.

3.3.4 Gain/Channel Register (base + 85H)

The AIO module uses a 32-element onboard Gain RAM to store a gain factor for each analog input channel. One of three gain ranges is selected via jumper-option at the time the module is installed (refer to Chapter 2, Section 2.7.5). For convenience, the gain ranges and the gain factors covered by each range are shown again in Table 3-3.

Table 3-4. Input Gain Ranges

Gain Range	Gain Factors Covered
Range 1 (x1)	1, 2, 5, or 10
Range 2 (x4)	4, 8, 20, or 40
Range 3 (x10)	10, 20, 50, or 100

Immediately after power-up or system reset, the Gain RAM should be programmed (initialized) to provide each input channel (16 differential channels or 32 single-ended channels) with an associated gain factor. Once an input channel is initialized in this fashion, the associated gain factor will automatically be applied when any A/D conversion occurs on that channel.

The Gain RAM is programmed by using the Gain/Channel Register (base + 85H). If the module is operating in the Random Channel Conversion Mode (refer to Section 3.4.1), this register may also be used to "force" start an A/D conversion (much like the function performed by Bit D7 of the Status/Control Register). Figure 3-3 shows how the Gain/Channel register is arranged.

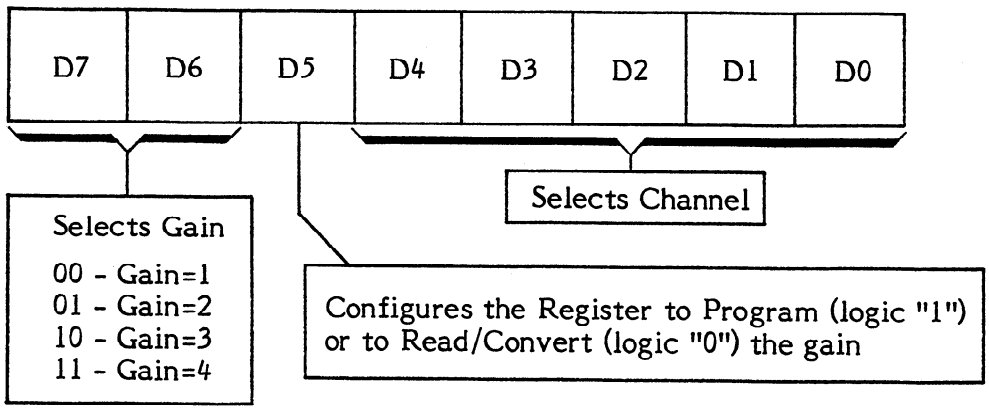


Figure 3-3. Gain/Channel Register

The first five bits of this register (D0-D4) are used to select one of the analog input channels (0-15 differential, 0-31 single-ended) for channel conversion or channel gain programming. Table 3-5 lists the channel selection codes which would be used for differential (0-15) and single-ended (0-31) operation.

Table 3-5. Channel Selection Codes

Data Bits					Channel Selected
D4	D3	D2	D1	D0	
0	0	0	0	0	Chan. 0
0	0	0	0	1	Chan. 1
0	0	0	1	0	Chan. 2
0	0	0	1	1	Chan. 3
0	0	1	0	0	Chan. 4
0	0	1	0	1	Chan. 5
0	0	1	1	0	Chan. 6
0	0	1	1	1	Chan. 7
0	1	0	0	0	Chan. 8
0	1	0	0	1	Chan. 9
0	1	0	1	0	Chan. 10
0	1	0	1	1	Chan. 11
0	1	1	0	0	Chan. 12
0	1	1	0	1	Chan. 13
0	1	1	1	0	Chan. 14
0	1	1	1	1	Chan. 15
1	0	0	0	0	Chan. 16
1	0	0	0	1	Chan. 17
1	0	0	1	0	Chan. 18
1	0	0	1	1	Chan. 19
1	0	1	0	0	Chan. 20
1	0	1	0	1	Chan. 21
1	0	1	1	0	Chan. 22
1	0	1	1	1	Chan. 23
1	1	0	0	0	Chan. 24
1	1	0	0	1	Chan. 25
1	1	0	1	0	Chan. 26
1	1	0	1	1	Chan. 27
1	1	1	0	0	Chan. 28
1	1	1	0	1	Chan. 29
1	1	1	1	0	Chan. 30
1	1	1	1	1	Chan. 31

The upper two bits of the register (D6 and D7) are used to select one of the four gain factors available in each of the three jumper-selectable gain ranges (refer to Table 3-4). Table 3-6 shows which codes are written to bits D6 and D7 to select specific gain factors, depending upon which of the three gain ranges has been previously jumper-selected.

Table 3-6. Gain Selection Bits

Gain/Channel Register		Gain Selected		
D7	D6	Range 1	Range 2	Range 3
0	0	1	4	10
0	1	2	8	20
1	0	5	20	50
1	1	10	40	100

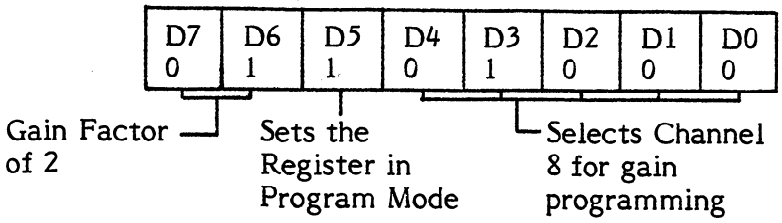
The state of the sixth bit (d5) of the Gain/Channel Register allows the register to be used to program (initialize) the Gain RAM, or it allows the register to be used to read the Gain RAM. By writing a logic "1" to this bit, together with a specific channel number (bit D0-bit D4), and the desired gain factor (bit D6 & D7) from the selected gain range, the specified channel will be programmed to apply the chosen gain factor any time it converts a signal. By writing a logic "0" to bit D5 of the Gain/Channel Register, together with a specific channel number, the corresponding gain factor (previously programmed) can b read back from bits D6 and D7.

In addition, if the module is operating in the Random Channel Conversion Mode (refer to Section 3.4.1) an A/D conversion will be initiated on the specified channel when the channel gain is read by the preceeding method. Thus, by writing a logic "0" to bit D5, together with a specific channel number, a conversion can be "forced" on the specified channel.

The following examples show how writing a specific byte to the Gain/Channel Register will program a gain of 2 for channel 8 (Example 1), and another byte will read a (previously) programmed gain on channel 15, and initiate a conversion (Example 2). Both examples assume that the gain range was jumper-configured for range 1.

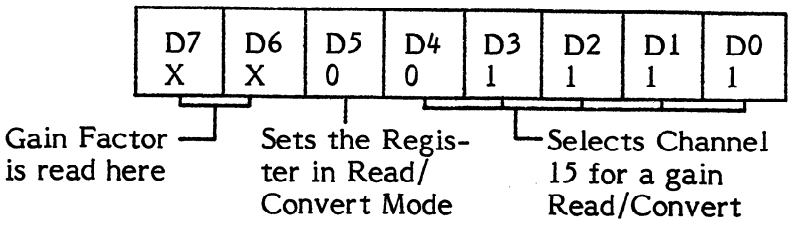
Example 1:

By writing 68H to the module base address + 85H, analog input channel 8 would be programmed for an automatic application of a gain factor of 2 when it converts a signal.



Example 2:

By writing 0FH to the module base + 85H (in the Random Channel Mode), the Gain RAM for channel 15 can be read (the gain is read at bits D6 and D7). In addition a conversion is initiated on channel 15.



3.3.5 A/D Data Input Register (base + word location 86H)

The A/D converter produces digital data, which corresponds with the applied analog input from a specified channel. This digital data is accessible to the "Host" processor at the 16-bit A/D Data Input Register (base + 86H). A 16-bit (word) register is utilized to provide the space necessary for 12-bit resolution. The digital information in this register may be read in either the byte or word format. However, when reading the A/D input data in the byte format, it is necessary to read the high byte (base + 86H) before the low byte (base + 87H). This stipulation is mandatory, due to the fact that when the module is operating in either sequential or single channel conversion mode, a read from the low data byte (base + 87H) will initiate a new A/D conversion, and will thus write over the information contained in the high-order byte.

Figure 3-4 shows the format of the A/D data input register.

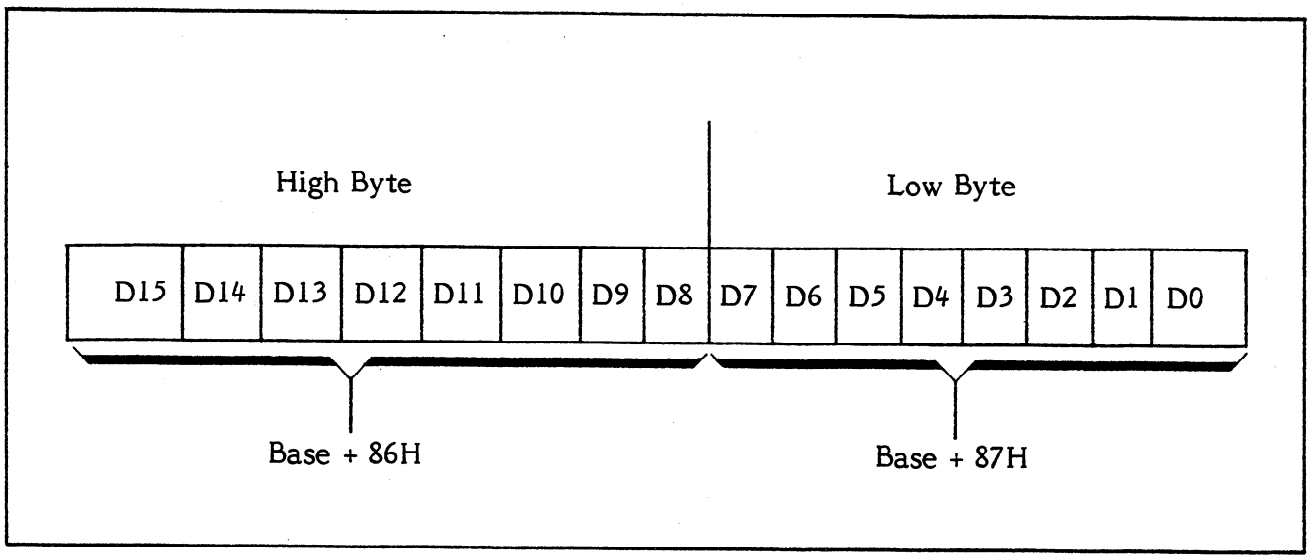


Figure 3-4. A/D Data Input Register

The manner in which data appears at the A/D Data Register is entirely dependent upon which input operation mode has been previously programmed (refer to Section 3.4 and the explanation of Status/Control bits D5 and D6 in Section 3.3.2.1 for information on the analog input modes).

3.3.5.1 A/D Data Format

The A/D converter digitizes the value of an analog signal on the input of a selected channel. The digital format of the converted data depends upon which data format and input voltage mode (unipolar or bipolar) have been previously jumpered during module installation (refer to Sections 2.7.1 and 2.7.3).

The analog input signals can be divided into two general groups: unipolar input, where the input has only positive polarity (e.g., 0-5V); and bipolar input, where the input magnitude can "swing" between a positive and a negative polarity (e.g., +5V to -5V).

If the inputs are configured to accept unipolar voltages, the straight binary format of data encoding is usually selected. If the inputs are configured to accept bipolar voltages, the data can be encoded in either offset or two's complement (to encompass handling negative numbers). The three formats are listed in the following tables.

Table 3-7. Unipolar Mode
(Straight Binary Encoding)

Straight Binary: D15															D0	Analog Input
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Vfsr - 1LSB
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1/2 Vfsr
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0V

Table 3-8. Bipolar Modes
(Offset Binary or Two's Complement)

Offset Binary: D15															D0	Analog Input
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	Vfsr - 1LSB
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1/2 (+Vfsr)
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0V
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1/2 (-Vfsr)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-Vfsr
Two's Complement: D15															**D0**	**Analog Input**
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	Vfsr - 1LSB
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1/2 (+Vfsr)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0V
1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1/2 (-Vfsr)
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	-Vfsr

NOTE

The "LSB" (Least Significant Bit) represents the change in input voltage that causes an increase or decrease of the binary code by one bit. The "LSB" is derived from the full scale voltage range (Vfsr) divided by the maximum conversion resolution (i.e., 12 bits or 4096 in binary equivalent). Thus, the value of one LSB can be determined by the following:

$$\text{Unipolar LSB} = \frac{\text{Vfsr}}{4096} \qquad \text{Bipolar LSB} = \frac{(+\text{Vfsr}) - (-\text{Vfsr})}{4096}$$

3.3.6 D/A Data Registers (base + word locations 88H, 8AH, 8CH, and 8EH)

The D/A converter can produce either a voltage or a current output for any of four available output channels. The output channels are independently jumper-configured for the type of output required (refer to Section 2.6.3). The value of the analog output will be a fraction of the converter's "full scale" output, defined by the digital code sent to the converter.

The data to be converted is sent to one of the four D/A conversion channels by writing to the module base + the offset for the desired channel. Figure 3-5 shows relative positions of the four output channels within the I/O Interface Block.

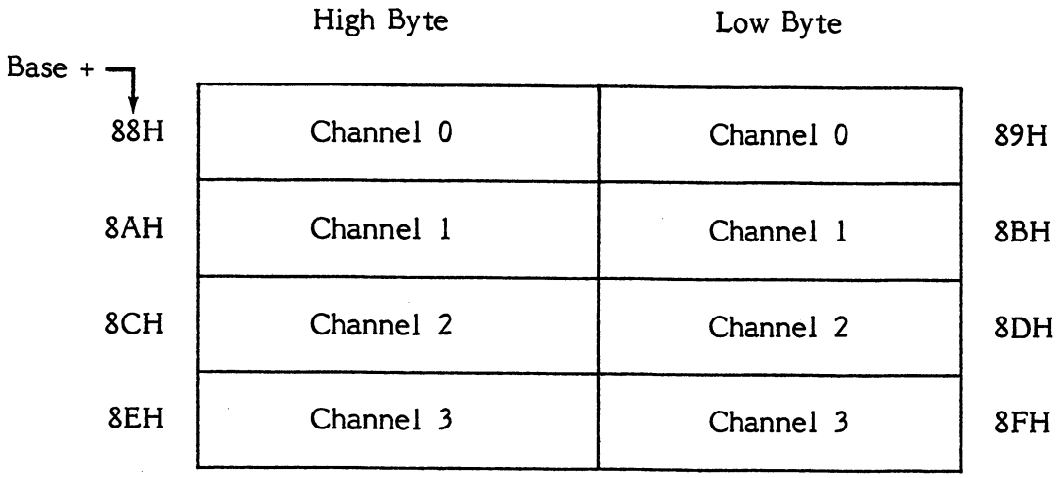


Figure 3-5. D/A Data Output Registers

The digital to analog conversion process begins when data is written to the low order byte of an output register. For this reason, either an entire word must be written to the data port, or, if one byte is written at a time, the high order byte must be written before the low order byte. Whenever the low order byte is written, the last high order byte written will be used as data for the D/A conversion.

3.3.6.1 Digital Output Data Format

The digital data written to the D/A Registers corresponds to the magnitude of the analog output signal in a relation that is different for each of two digital data formats (i.e., Straight Binary Encoding, or Offset Binary Encoding).

The analog output signals can be divided into two general groups; Unipolar output, where the output has only positive polarity (e.g., 0-5V), and Bipolar output, where the output magnitude can have a negative or positive polarity (e.g., $\pm$5V). Current mode is unipolar. The formats are listed in the following tables.

In the unipolar mode, the data to be converted must be encoded in the Straight Binary form (see Table 3-9).

Table 3-9. Unipolar Mode
(Straight Binary Encoding)

X = Don't Care Voltage Mode: D15 D0	Analog Input
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	+Vfsr
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	1/2 Vfsr
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	0V
Current Mode: D15 D0	**Analog Output 4-20mA**
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	20mA - 1LSB
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	12mA
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	4mA

In the bipolar mode, the digital value converted to analog is usually encoded in offset binary form. In offset binary encoding, the negative full scale voltage (-Vmax) is represented by all binary zero's. The positive full scale voltage (minus one LSB) is represented by all binary one's. Thus, the voltage scale represented is "offset" by a factor of the full scale voltage "swing" (+Vmax to -Vmax). Table 3-10 shows the offset and the two's complement mode of encoding.

Table 3-10. Bipolar Modes

X = Don't Care Bipolar Offset Encoding: D15 D0	Analog Input
X X X X 1 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1LSB
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	1/2 Vfsr
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	1/2 (-Vfsr)
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	-Vfsr
Two's Complement Encoding: D15 D0	**Analog Output 4-20mA**
X X X X 0 1 1 1 1 1 1 1 1 1 1 1	+Vfsr - 1LSB
X X X X 0 1 0 0 0 0 0 0 0 0 0 0	1/2 (+Vfsr)
X X X X 0 0 0 0 0 0 0 0 0 0 0 0	0V
X X X X 1 1 0 0 0 0 0 0 0 0 0 0	1/2 (-Vfsr)
X X X X 1 0 0 0 0 0 0 0 0 0 0 0	-Vfsr

NOTE

The "LSB" (Least Significant Bit) represents the change in output voltage (or current) that causes an increase or decrease of the binary code by one bit. The "LSB" is derived from the full scale range of either current or voltage (Vfsr) divided by the maximum conversion resolution (i.e., 12 bits or 4096 in binary equivalent). Thus, the value of one LSB can be determined by the following:

$$\text{Unipolar LSB} = \frac{Vfsr}{4096} \qquad \text{Bipolar LSB} = \frac{(+Vfsr) - (-Vfsr)}{4096}$$

$$\text{Current LSB} = \frac{20mA - 4mA}{4096}$$

3.4 A/D CONVERSION PRINCIPLES

A general procedure for configuring the AIO Module to convert analog inputs to digital data must include the following elements:

1. Configure jumpers and switches (refer to Chapter 2) for the desired interrupt level, input type (differential or single-ended, and bipolar or unipolar), input voltage range, input gain range, and input binary data format.

2. Initialize (program) Gain RAM by writing to the Gain/Channel Register (refer to Section 3.3.4).

3. Perform calibration (see Chapter 4).

4. Select one of the four A/D conversion modes by writing to the Status/Control Register (refer to Section 3.3.2.1 and Section 3.4.1).

5. Initiate the A/D conversion process (a conversion may be: "force" started, initiated by reading the low order byte of the A/D Data Register in two of the four modes, or started via an external trigger).

3.4.1 A/D Conversion Modes

The A/D conversion process may operate in any one of four possible conversion modes. They are:

MODE	DEFINITION
0	Single Channel Conversion - Repeated A/D conversions are performed on a specified channel.
1	Sequential Channel Conversion - Channels are converted in sequence, beginning with a specified channel.
2	Random Channel Conversion - A Single A/D conversion is performed on the selected channel.

3 Externally Triggered Conversion - A selected channel will be converted only when a positive trigger signal (referenced to power ground) is received on Pin 50 (ground reference on Pin 49) of connector JK1.

A conversion mode is selected by writing its corresponding two-bit code to bits D5 and D6 of the Status/Control Register (refer to Table 3-2 -- Input Mode Options). The following subsections define each of the input conversion modes and list the procedure for using each.

3.4.1.1 Single Channel Mode

In the Single Channel Mode, the module will automatically start another conversion on the specified channel, after the low order A/D input byte (base + 87H) has been read. An added feature of the Single Channel Mode is that it converts 50% faster than the other three modes (i.e., 25uS as opposed to 50uS).

Procedure

1) Write a control byte to the Status/Control register (base + 81H) that sets bits D5 and D6 both to logic "0".

2) Select the desired channel by writing the channel number to bits D0-D4 of the Gain/Channel Register (base + 85H). Assuming that the corresponding Gain RAM was properly initialized (programmed) after power-up, the gain will not have to be rewritten at this time (unless a change in gain is desired).

3) To initiate the first conversion, perform a "dummy" read (base + 87H), or force a conversion by writing a logic "1" to bit D7 of the Status/Control Register.

4) Wait until the conversion is complete (i.e., check the busy flag (bit D7) of the Status/Control Register, or use interrupts).

5) Read the results of the conversion from the A/D input register -- high byte (base + 86H) before low byte (base 87H), or perform a 16-bit read. After the low byte is read, a new conversion will automatically be initiated on the same channel.

3.4.1.2 Sequential Channel Mode

In the Sequential Channel Mode, the module will automatically increment the channel number by one and initiate a conversion on the next (previous channel + 1) channel, after the low order A/D input byte (base + 87H) has been read. A conversion can be initiated in this mode without incrementing the channel number by writing a logic "1" to bit D7 of the Status/Control register (i.e., by forcing a conversion).

Procedure

1) Write a control byte to the Status/Control Register (base + 81H) that sets bit D5 to logic "1" and bit D6 to logic "0".

2) Select a starting channel by writing the channel number to bits D0-D5 of the Gain/Channel Register (base + 85H). Assuming that the corresponding Gain RAM

was properly initialized (programmed) after power-up, the gain will not have to be rewritten at this time (unless a change in gain is desired).

3) To initiate the first conversion, write a control byte to the Status/Control Register that sets bit D7 to logic "1". This action will "force" a conversion on the specified starting channel without incrementing the channel number. Then, by reading the low order A/D data byte (base + 87H0), the channel number will be incremented by one and the next conversion will be started.

NOTE

The first conversion may also be initiated by doing a "dummy" read of the low order A/D input byte, but this method will increment the channel number by one prior to the conversion. Thus the first channel number converted will be one more than the channel number written to the Gain/Channel Register in step 2. When the "dummy" read method is used to initiate the first conversion, the channel "offset" may be corrected by specifying a channel number (in step 2) which is one less than the desired starting channel number (e.g., if the first channel you wish to convert is channel 0 then channel 31 should be entered as the starting channel).

4) Wait until the conversion is complete (i.e., check the busy flag (bit D7) of the Status/Control Register, or use interrupts).

5) Read the results of the conversion from the A/D data registers -- high byte (base + 86H) before low byte (base + 87H), or perform a 16-bit read. After the low byte is read, a new conversion will automatically be initiated on the next (previous channel + 1) channel.

3.4.1.3 Random Channel Selection

In the Random Channel Mode, a control byte written to the Gain/Channel Register which specifies a channel number and sets bit D5 to logic "0" will automatically start a conversion on the specified channel.

Procedure

1) Write a control byte to the Status/Control Register that sets bit D5 to logic "0" and bit D6 to logic "1".

2) Select the desired channel and initiate the conversion by writing the channel number to bits D0-D4, and a logic "0" to bit D5 of the Gain/Channel Register. Assuming that the corresponding Gain RAM was properly initialized (programmed) after power-up, this action will initiate a conversion with the correct gain on the specified channel. A conversion may also be forced by using bit D7 of the Status/Control Register.

3) The result of the conversion can be read from the A/D data registers (base + 86H - 87H) in either the byte or word format. In the Random Channel Mode, the data resulting from a conversion will remain in the A/D registers until another conversion is initiated.

3.4.1.4 Externally Triggered Conversion Mode

This mode allows the rising edge of a low-going, externally triggered pulse (on pin 50 of JK1), referenced to power ground (Pin 49 of JK1), to initiate a conversion. Figure 3-6 shows the timing constraints.

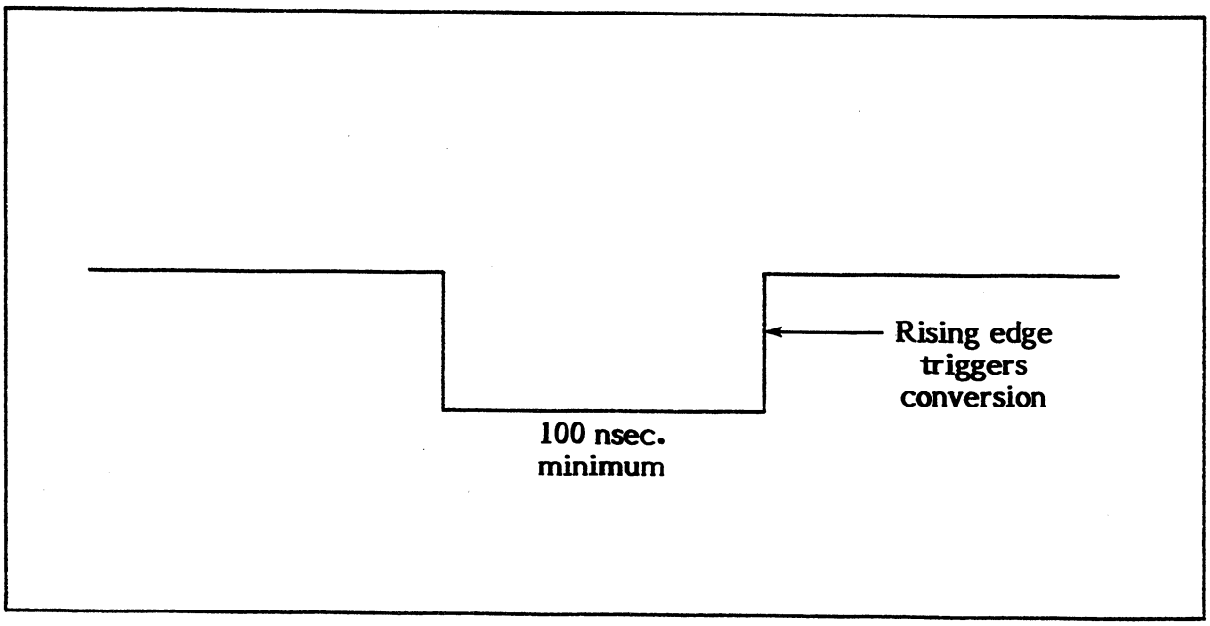


Figure 3-6. External Trigger Pulse

Procedure

1) Connect the external trigger source to pin 50 of connector JK1, and connect the external trigger source return to pin 49 of connector JK1.

2) Write a control byte to the Status/Control Register (base + 81H) that sets bits D5 and D6 both to logic "1".

3) Select the desired channel by writing the channel number to bits D0-D4 of the Gain/Channel Register. Assuming that the Gain RAM was properly initialized (programmed) after power-up, it will not be necessary to rewrite the gain at this time (unless a gain change is required).

4) The selected channel will initiate a conversion on the rising edge of the external trigger. The conversion results are read from the A/D data registers. The next conversion will not take place until the next rising edge of the external trigger, or until a new conversion is "forced" on the channel by using bit D7 of the Status/Control Register.

NOTE

A software reset (refer to Section 3.3.2.1) will reset the flip-flop used to latch the external trigger pulse, and thus abort any conversion in progress.

If an external trigger occurs while the module is operating in any mode other than the external trigger mode, the trigger signal will be latched and a conversion will occur as soon as the external trigger mode is entered.

3.4.2 Interrupts

The analog input portion of the module can generate an interrupt to notify the host that the A/D conversion is complete and the results are available. The level and vector generated by this interrupt are both user-selectable.

The following three steps must be performed in order to generate an interrupt:

1) Interrupt level select switches must be set for the desired level (I1-I7) and jumpers J1 and J3 must be configured to enable the module IACK* handling circuitry (refer to Section 2.4 of Chapter 2).

2) Interrupts must be enabled via bit D2 in the Status/Control Register (refer to Section 3.3.2.1).

3) The Interrupt Vector Register (location base + 83H) must be loaded with the required vector. This vector register will be read by the interrupt handler when the interrupt is acknowledged.

At the completion of a conversion, an interrupt will be generated.

3.4.3 Current Loop Inputs

An A/D input will operate in a 4-20mA or 10-50mA current loop configuration with the addition of an external current sensing resistor. The current sensing resistor should be selected to generate a voltage within the predetermined, jumper-selected voltage range (0-10V max.). A voltage drop of less than 1V will provide current of less than 4mA, and would thus indicate that the current loop was not operating properly. Typically, the resistors used would be a 500 Ohm 1/2W for the 4-20mA configuration, and a 200 Ohm 1/2W for the 10-50mA configuration. The resistors used should be 0.1% tolerance or better, with stable temperature coefficient characteristics (e.g., 25ppm or better). All input channels operate with the same full scale input range.

3.5 D/A CONVERSION PRINCIPLES

A general procedure for configuring the AIO Module to convert digital data to analog outputs must include the following elements:

1) Configure jumpers and switches (refer to Chapter 2) for output type (voltage or current), output voltage range (unipolar or bipolar), digital data conversion format (straight binary or offset binary), and D/A converter reset state at power-up or system reset (i.e., the converters are loaded with either all logic "0's" or all logic "1's" at power-up or reset).

2) Perform Calibration (see Chapter 4).

3) Write the conversion data to the desired 16-bit D/A output register in either the byte or word mode. If the data is transferred to the register in the byte mode, the high order byte must be written prior to the low order byte. When the low order byte is written, the D/A conversion is initiated and the output will change state.

Thus, initiating conversions on the D/A output channels is simply a matter of writing the binary conversion data to the module base address + (word locations) 88H, 8AH, 8CH, and 8EH.

3.5.1 Current Loop Outputs

When the outputs are configured for current loop operation (see Section 2.6.3), the loop supply voltage is provided by an on-board 15V DC-DC converter. This converter not only generates ±15V from the VMEbus supplied +5V, but it serves to separate the analog ground from the digital ground. In addition, the module has its own precision voltage source to provide an internal reference voltage. The D/A outputs are capable of handling current loop configurations in the 4-20mA range.

When used in the current output mode, the output channels must be jumpered for the 0 to 10V output range (refer to Table 1-10).

Chapter 4

CALIBRATION

4.1 INTRODUCTION

Calibration facilities have been provided on the AIO Module for both the analog input and the analog output circuits. The module is calibrated in the ±10V A/D input voltage range and the 0-10V D/A output voltage range before it leaves the factory; however, it is recommended that if the module is configured to operate in ranges other than these, the calibration should be checked and adjusted if necessary. As a general rule, the input/output circuitry should be recalibrated whenever voltage range jumpers and voltage/current select jumpers are changed.

The calibration procedure is divided into two parts; input circuit calibration and output circuit calibration. Input circuit calibration entails offset nulling the instrumentation amplifier, and offset adjusting and gain adjusting the A/D converter. Output calibration entails offset and gain adjustment for each output channel in either the unipolar or the bipolar modes of operation. Tables 4-1 and 4-2 provide the lists of the potentiometers and their applications for both A/D and D/A calibration. Relative locations of the calibration potentiometers can be found in Figure 2-1.

Table 4-1. A/D Calibration Potentiometers

Resistor No.	Type of Adjustment
R3	Offset for A/D converter
R5	Gain for input circuit
R64	Programmable gain amp offset

Table 4-2. D/A Calibration Potentiometers

Resistor No.	Type of Adjustment
R10	Gain for CH 3
R12	Gain for CH 2
R14	Gain for CH 1
R16	Gain for CH 0
R20	Ch 3 bipolar offset
R21	CH 2 bipolar offset
R22	CH 1 bipolar offset
R23	CH 0 bipolar offset
R26	CH 3 unipolar offset
R29	CH 2 unipolar offset
R32	CH 1 unipolar offset
R25	CH 0 unipolar offset

4.2 INPUT CALIBRATION

Equipment Required:

1) A 5-digit volt meter capable of reading ±30uV.
2) A small flat-bladed screw driver.
3) A precision voltage source capable of supplying 1.22mV ±30uV.

The inputs can be calibrated in either the single-ended or differential configuration. Calibration begins by offset nulling the instrumentation amplifier with channel 0 selected and its inputs grounded.

Programmable Gain Offset Adjustment

1) Remove any connectors at JK1.

2) Set potentiometer R64 to center position, and insert jumper J45 (channel 0) if in single-ended mode, or insert jumper J44 and jumper J45 if in differential mode (channel 0 HI and channel 0 LO). (Note: If the module is in single-ended mode, jumper J44 shorts channel 8 to ground.)

3) Set input to address the first channel (CH 0).

4) Insert jumpers J22A and J22B, and set the input stage gain to 1 (by setting bits D6 and D7 of the Gain/Channel Register to logic "0"). Measure and record the output voltage (VI) of the instrumentation amp at TP2 (TP1 is ground).

5) Set the input stage gain to 10 (by setting bits D6 and D7 of the Gain/Channel register to logic "1"). Measure and record the output voltage (VO) at TP2.

6) Calculate the voltage offset with the following formula:

   Voltage Offset (Voos) = 1/9 * ((10 * VI) - VO)

7) While maintaining an input stage gain of 10, adjust the input offset voltage potentiometer (F64) until the output at TP2 is equal to Voos (±30uV).

8) Reset jumpers on J22 for the desired gain range as depicted in Table 2-14.

9) Remove grounding jumpers J44/J45.

A/D Offset and Gain Adjustment

With the previous networks nulled and J22 set to the desired gain range, it is necessary to perform continuous conversions on channel 0 (channel 0 must be set for the highest programmable gain factor; i.e., bits D6 and D7 of the Gain/Channel Register must be set to logic "1"). The conversion result should be displayed on a CRT on HEX format for verification purposes. Perform the following setps:

1) Using a precision voltage source, apply 1.22mV ±30uV to channel 0.

2) Adjust the offset potentiometer R3 until the conversion result toggles between the two transition points described in Table 4-3.

Table 4-3. Calibration Points

Analog Input	Transition Points			
	0V +	1/2LSB	Full Scale -	1 1/2LSB
Unipolar (straight binary)	0000H	0001H	0FFEH	0FFFH
Bipolar (offset binary)	0800H	0801H	0FFEH	0FFFH
Bipolar (two's complement offset binary)	0000H	0001H	07FEH	07FFH

Perform the following steps to adjust the gain:

1) Apply the full scale voltage of the selected range minus 1 1/2LSB. Table 4-4 shows the voltages to apply for each range (assuming a gain of 1).

Table 4-4. Full Scale Voltage Factors

Full Scale Voltage Ranges	Full Scale Range Minus 1-1/2 LSB
±10V	9.993V
0-10V	9.996V
±5V	4.996V
0-5V	4.998V
±2.5V	2.498V

2) Adjust potentiometer R5 until the result toggles between the two transition points in Table 4-3.

NOTE

After completing input calibration, make sure that grounding jumpers J44 and J45 are removed.

4.3 OUTPUT CALIBRATION

Equipment Required:

1) A 5-digit volt meter capable of reading ±30uV.
2) A small flat-bladed screw driver.

Output calibration entails voltage offset adjustment, and gain adjustment for each channel, in both the unipolar and bipolar configurations. For unipolar operation,

potentiometers R35, R32, R29, and R26 are adjusted for channels 0 through 3 respectively. Bipolar operation requires that potentiometers R23, R22, R21, and R20 be adjusted for channels 0 through 3 respectively. Potentiometers R16, R14, R12, and R10 are used to adjust the gain on channels 0 through 3 respectively.

Table 4-5 shows which potentiometers relate to which output channels.

Table 4-5. Output Offset Adjustment Potentiometers

Unipolar	Bipolar	Gain	Corresponding Channel
R35	R23	R16	CH 0
R32	R22	R14	CH 1
R29	R21	R12	CH 2
R26	R20	R10	CH 3

Unipolar Offset Adjustment

1) Set jumpers J26, J30, J34, or J38 to the "B" position, dependent upon which channels are to be offset adjusted.

2) Turn all bits off (load binary zeros) to the channel being calibrated.

3) Make sure that the channel is jumpered for voltage output (J39-J42).

4) Adjust the (unipolar) potentiometer that corresponds to the channel being calibrated until the output reads 0.0000 volta $\pm$30uV.

5) Turn all bits on (FFFH) to the channels being calibrated.

6) Adjust the corresponding gain potentiometer until the output is 9.9976 volts (i.e., 1 LSB less than the nominal full scale of 10.000 volts).

Steps 2, 3, and 5 may also be executed with the channels configured for current output. In this case, the channel offset potentiometer is adjusted for an output of 4mA (or 1.000V $\pm$30uV across a 250 Ohm, 0.1% resistor returned to the -13V (-IOUT) pin on connector JK2), and the gain potentiometer should be adjusted for an output of 20mA (or 5.000 volts).

NOTE

Make certain that the resistor used does not change value due to self-heating.

Bipolar Offset Adjustment

1) Set jumpers J26, J30, J34, or J38 to the "A" position, dependent upon which channel(s) are to be offset adjusted.

2) Turn all bits off (load binary zero's) to the output channel being calibrated.

3) Adjust the (bipolar) potentiometer that corresponds to the channel being calibrated until the output reads -5.00 ±30uV.

4) Turn all bits on (load FFFH) to the output channel being calibrated.

5) Adjust the gain potentiometer until the output reads +4.9976.

Appendix A

XYCOM STANDARD I/O ARCHITECTURE

INTRODUCTION

The purpose of this Appendix is to define XYCOM's Standard I/O Architecture for XVME I/O modules. This Standard I/O Architecture has been incorporated on all XVME I/O modules in order to provide a simpler and more consistent method of programming for the entire module line. The I/O Architecture specifies the logical aspects of bus interfaces, as opposed to the "physical" or electrical aspects as defined in the VMEbus specifications. The module elements which are standardized by the XYCOM I/O Architecture are the following:

1. Module Addressing -- Where a module is positioned in the I/O address space and how software can read from it or write to it.

2. Module Identification -- How software can identify which modules are installed in a system.

3. Module Operational Status -- How the operator can (through software) determine the operational condition of specific modules within the system.

4. Interrupt Control -- How software is able to control and monitor the capability of the module to interrupt the system.

5. Communication between Modules -- How master (host) processors and intelligent I/O modules communicate through shared global memory or the dual-access RAM on the I/O modules.

6. The I/O Kernel -- How intelligent and non-intelligent "kernels" facilitate the operation of all XYCOM I/O modules.

MODULE ADDRESSING

The XYCOM I/O Architecture Design Specification recommends that XVME modules should be addressed within the VMEbus-defined 64K short I/O address space. The restriction of I/O modules to the short I/O address space provides separation of program/data address space and the I/O address space. This convention simplifies software design and minimizes hardware and module cost, while at the same time, providing 64K of address space for I/O modules.

Base Addressing

Since each I/O module connected to the bus must have its own unique base address, the base addressing scheme for XYCOM VME I/O modules has been designed to be jumper/switch-selectable. Each XVME I/O module installed in the system requires at least a 1K byte block of the short I/O Address Space. Thus, each I/O module has a base address which starts on a 1K boundary. As a result, the XYCOM I/O modules

have all been implemented to decode base addresses in 1K (400H) increments. Figure A-1 shows an abbreviated view of the short I/O memory.

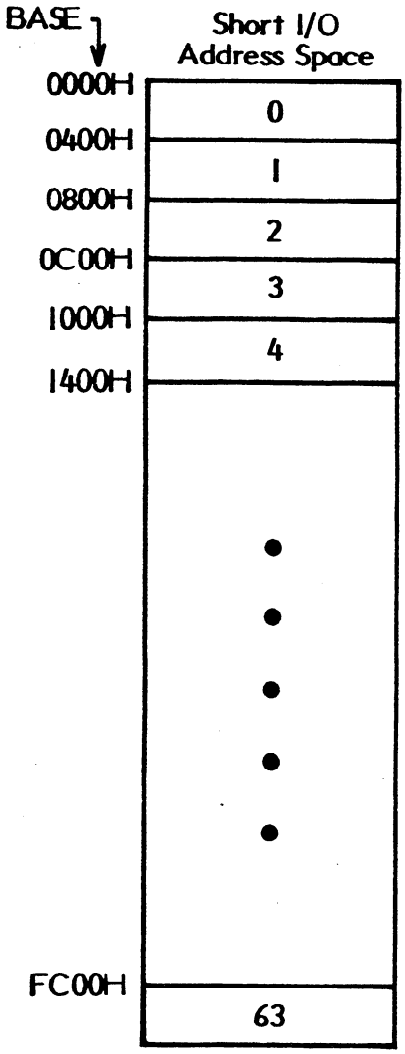


Figure A-1. 64K Short I/O Address Space for Modules Which Occupy a 1K Block

Standardized Module I/O Map

The block of short I/O addresses (called the I/O Interface Block) allocated to each XVME module is mapped with a standardized format in order to simplify programming and data access. The locations of frequently used registers and module-specific identification information are uniform. For example, the module identification information is always found in the first 32 odd bytes of the module memory block -- with these addresses being relative to the jumpered base address (i.e., Module I.D. data address = base address + odd bytes 1H - 3FH). The byte located at base address+81H on each module contains a Status/Control register which provides the results of diagnostics for verification of the module's operational condition. The next area of the module I/O Interface Block (base address + 82H - up to FFFH) is module-specific and it varies in size from one module to the next. It is in this area that the module holds specific I/O status, data, and pointer registers for use with IPC protocol. All intelligent XVME I/O modules have an area of their I/O Interface Blocks defined as "dual access RAM." This area of memory provides the space where XVME "slave" I/O modules access their command blocks and where XVME "master" modules could access their command blocks (i.e., "master" modules can also access global system memory).

The remainder of the I/O Interface Block is then allocated to various module-specific tasks, registers, buffers, ports, etc.

Figure A-2 shows an address map of an XVME I/O module interface block, and how it relates to the VMEbus short I/O address space. This example shows an I/O Interface Block which occupies a 1K segment of short I/O Address Space. It should be noted that some modules (the XVME-164 MBMM for example) will occupy up to a 4K segment of short I/O Address Space. Notice that any location in the I/O Interface Block may be accessed by simply using the address formula:

Module Base Address + Relative Offset = Desired Location

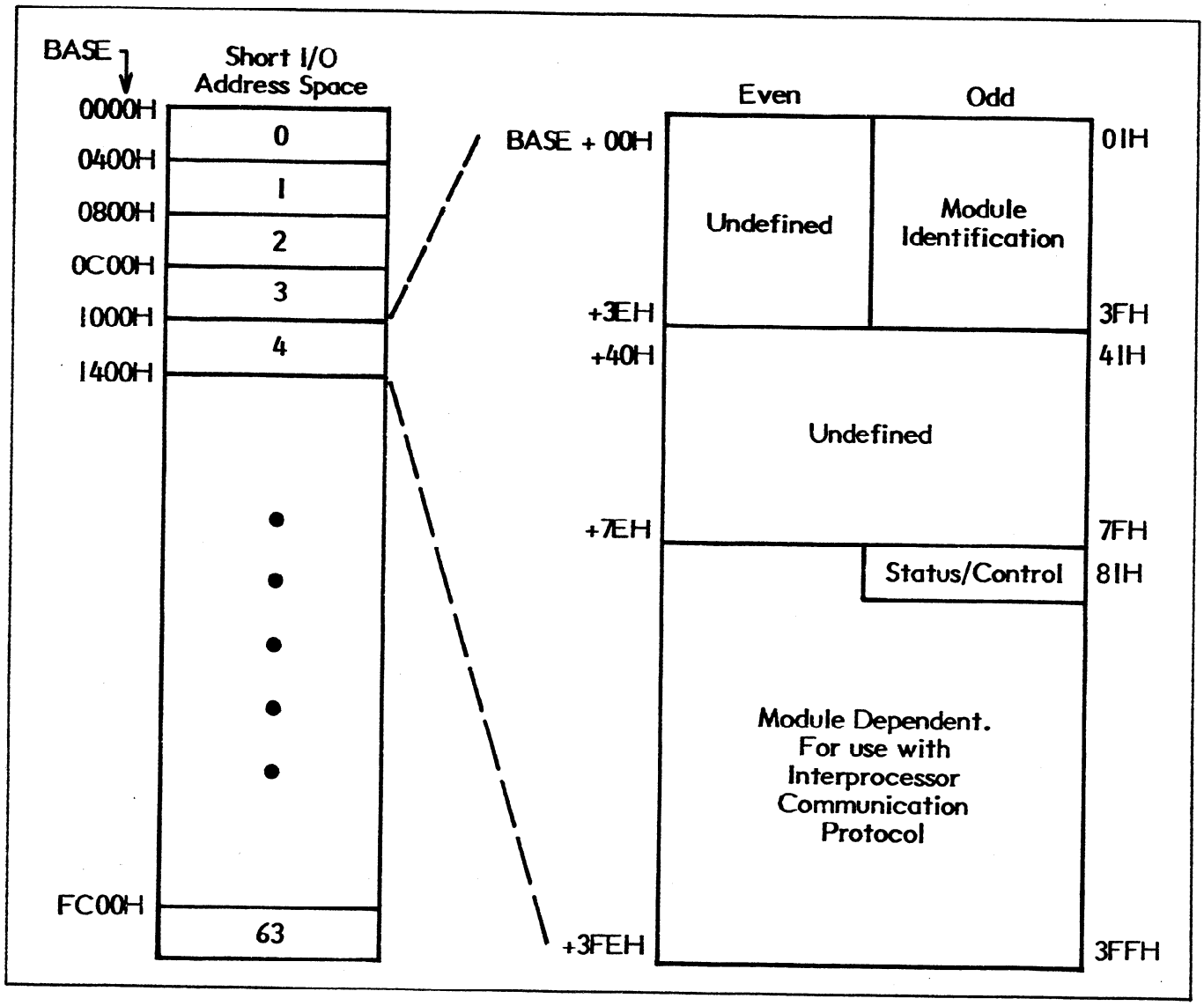


Figure A-2. XVME I/O Module Address Map

MODULE SPECIFIC IDENTIFICATION DATA

The module identification scheme provides a unique method of registering module specific information in an ASCII encoded format. The I.D. data is provided as thirty-two ASCII encoded characters consisting of the board type, manufacturer identification, module model number, number of 1K-byte blocks occupied by the module, and model functional revision level information. This information can be studied by the system processor on power-up to verify the system configuration and operational status. Table A-1 defines the Identification information locations.

Table A-1. Module I.D. Data

Offset Relative to Module Base	Contents	ASCII Encoding (in hex)	Descriptions
1	V	56	
3	M	4D	ID PROM identifier,
5	E	45	always "VMEID"
7	I	49	(5 characters)
9	D	44	
B	X	58	Manufacturer's I.D.,
D	Y	59	always "XYC" for XYCOM
F	C	43	modules (3 characters)
11	5	35	
13	4	34	Module Model Number
15	0	30	(3 characters and
17		20	4 trailing blanks)
19		20	
1B		20	
1D		20	
1F	1	31	Number of 1K byte blocks of I/O space occupied by this module (1 character)
21		20	Major functional revision
23	1	31	level with leading blank (if single digit)
25	1	30	Minor functional revision
27		20	level with trailing blank (if single digit)
29	Undefined		
2B	"		
2D	"		
2F	"		
31	"		
33	"		
35	"		Manufacturer
37	"		Dependent Information,
39	"		Reserved for future use
3B	"		
3D	"		
3F	"		

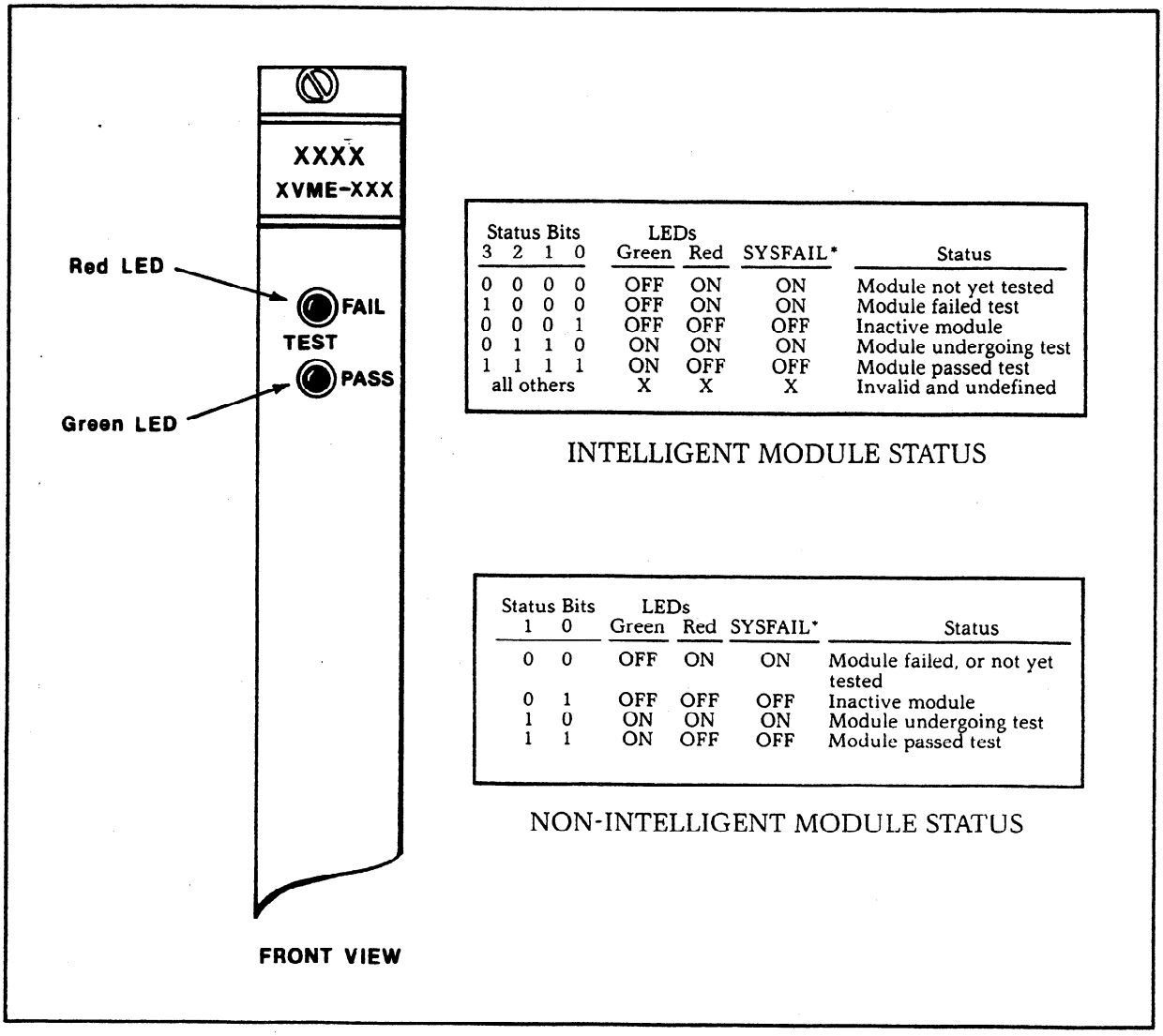
The module has been designed so that it is only necessary to use odd backplane addresses to access the I.D. data. Thus, each of the 32 bytes of ASCII data have been assigned to the first 32 odd I/O Interface Block bytes (i.e., odd bytes 1H-3FH).

I.D. information can be accessed simply by addressing the module base, offset by the specific address for the character(s) needed. For example, if the base address of the board is jumpered to 1000H, and if you wish to access the module model number (I/O interface block locations 11H, 13H, 15H, 17H, 19H, 1BH, and 1DH), you will individually add the offset addresses to the base addresses to read the hex-coded ASCII value at each location. Thus, in this example, the ASCII values which make up the module model number are found sequentially at locations 1011H, 1013H, 1015H, 1017H, 1019H, 101BH, and 101DH within the system's short I/O address space.

MODULE OPERATIONAL STATUS/CONTROL

All XVME intelligent I/O modules are designed to perform diagnostic self-tests on power-up or reset. For non-intelligent modules, the user must provide the diagnostic program. The self-test provision allows the user to verify the operational status of a module by either visually inspecting the two LEDs which are mounted on the module front panel (see Figure A-3), or by reading the module status byte (located at module base address + 81H).

Figure A-3 shows the location of the status LEDs on the module front panel. The two tables included with Figure A-2 define the visible LED states for the module test conditions on both the intelligent I/O modules and the non-intelligent I/O modules.



Status Bits 3	2	1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	0	0	OFF	ON	ON	Module not yet tested
1	0	0	0	OFF	ON	ON	Module failed test
0	0	0	1	OFF	OFF	OFF	Inactive module
0	1	1	0	ON	ON	ON	Module undergoing test
1	1	1	1	ON	OFF	OFF	Module passed test
all others				X	X	X	Invalid and undefined

INTELLIGENT MODULE STATUS

Status Bits 1	0	LEDs Green	Red	SYSFAIL*	Status
0	0	OFF	ON	ON	Module failed, or not yet tested
0	1	OFF	OFF	OFF	Inactive module
1	0	ON	ON	ON	Module undergoing test
1	1	ON	OFF	OFF	Module passed test

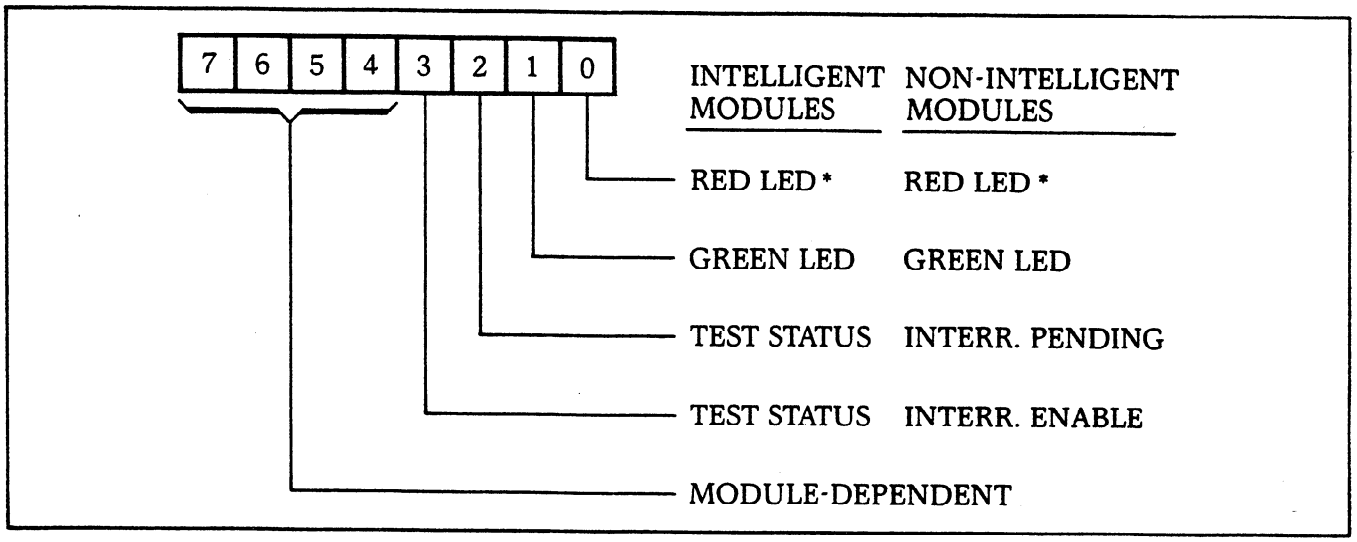
NON-INTELLIGENT MODULE STATUS

Figure A-3. Module LED Status

The module status/control register (found at module base address + 81H) on intelligent XVME I/O modules provides the current status of the module self-test in conjunction with the current status of the front panel LEDs. The status register on intelligent modules is a "Read Only" register and it can be read by software to determine if the board is operating properly.

On non-intelligent XVME I/O modules, the status/control register is used to indicate the state of the front panel LEDs, and to set and verify module generated interrupts. The LED status bits are "Read/Write" locations which provide the user with the indicators to accomodate diagnostic software. The Interrupt Enable bit is also a Read/Write location which must be written to in order to enable module-generated interrupts. The Interrupt Pending bit is a "Read Only" bit which indicates a module-generated pending interrupt.

Figure A-4 shows the status/control register bit definitions for both intelligent and non-intelligent XVME I/O modules.



Bit	Non-Intelligent Modules
0	Read/Write - Red LED 0 = Red LED On 1 = Red LED Off
1	Read/Write - Green LED 0 = Green LED Off 1 = Green LED On
2	Read Only - Interrupt Pending 0 = No Interrupt 1 = Interrupt Pending
3	Read/Write - Interrupt Enable 0 = Interrupts Not Enabled 1 = Interrupts Enabled
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Bit	Intelligent Modules
0	Read Only - Red LED 0 = Red LED On 1 = Red LED Off
1	Read Only - Green LED 0 = Green LED Off 1 = Green LED On
2 & 3	Read Only - Test Status Indicators Bit 3 / Bit 2 0 / 0 = Self-test not started 0 / 1 = Self-test in progress 1 / 0 = Self-test failed 1 / 1 = Self-test passed
4	Module dependent
5	Module dependent
6	Module dependent
7	Module dependent

Figure A-4. Status Register Bit Definitions

INTERRUPT CONTROL

Interrupts for non-intelligent modules can be enabled or disabled by setting/clearing the Interrupt Enable bit in the module status register. The status of pending on-board interrupts can also be read from this register. Interrupt control for intelligent modules is handled by the Interprocessor Communications Protocol.

Communications Between Processors

Communications between an intelligent "master" and an intelligent "slave" I/O module is governed by XYCOM's Interprocessor Communication (IPC) Protocol. This protocol involves the use of 20-byte Command Block data structures, which can be located anywhere in shared global RAM or dual-access RAM on an I/O module, to exchange commands and data between a host processor and an I/O module. Interprocessor Communication Protocol is thoroughly explained in Chapter 3 of this manual.

THE KERNEL

To standardize its XVME I/O modules, XYCOM has designed them around "kernels" common from module to module. Each different module type consists of a standard kernel, combined with module-dependent application circuitry. Module standardization results in more efficient module design and allows the implementation of the Standard I/O Architecture. The biggest benefit of standardization for intelligent modules is that it allows the use of a common command language or protocol (Interprocessor Communication Protocol in this case).

The intelligent kernel is based around either a 68000 microprocessor or a 68B09 microprocessor (on the XVME-164 MBMM). This design provides the full complement of VMEbus Requester and Interrupter options for master/slave interfacing, as well as all of the advantages provided by the various facets of the XYCOM Standard I/O Architecture (as covered earlier in this appendix).

The non-intelligent kernel provides the circuitry required to receive and generate all of the signals for a VMEbus defined 16-bit "slave" module. The non-intelligent kernel also employs the features of the XYCOM Standard I/O Architecture (as described earlier in this Appendix).

Appendix B

VMEbus CONNECTOR/PIN DESCRIPTION

The XVME-540 is physically configured as a non-expanded (NEXP), double-height, VMEbus compatible board. There is one 96 pin bus connector on the rear edge of the board, labelled P1 (refer to Chapter 3, Figure 3-1 for the locations). The pin connections for P1 contain the standard address, data, and control signals necessary for the operation of NEXP modules. P2 is used for power and ground.

Table B-1. P1 - VMEbus Signal Identification

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
ACFAIL*	1B: 3	AC FAILURE: Open-collector driven signal which indicates that the AC input to the power supply is no longer being provided or that the required input voltage levels are not being met.
IACKIN*	1A: 21	INTERRUPT ACKNOWLEDGE IN: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKIN* signal indicates to the VME board that an acknowledge cycle is in progress.
IACKOUT*	1A: 22	INTERRUPT ACKNOWLEDGE OUT: Totem-pole driven signal. IACKIN* and IACKOUT* signals form a daisy-chained acknowledge. The IACKOUT* signal indicates to the next board that an acknowledge cycle is in progress.
AM0-AM5	1A: 23 1B: 16,17, 18,19 1C: 14	ADDRESS MODIFIER (bits 0-5): Three-state driven lines that provide additional information about the address bus, such as size, cycle type, and/or DTB master identification.
AS*	1A: 18	ADDRESS STROBE: Three-state driven signal that indicates a valid address is on the address bus.
A01-A23	1A: 24-30 1C: 15-30	ADDRESS bus (bits 1-23): Three-state driven address lines that specify a memory address.

Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
A24-A31	2B: 4-11	ADDRESS bus (bits 24-31): Three-state driven bus expansion address lines.
BBSY*	1B: 1	BUS BUSY: Open-collector driven signal generated by the current DTB master to indicate that it is using the bus.
BCLR*	1B: 2	BUS CLEAR: Totem-pole driven signal generated by the bus arbitrator to request release by the current DTB master if a higher level is requesting the bus.
BERR*	1C: 11	BUS ERROR: Open-collector driven signal generated by a slave. It indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
BG0IN*-BG3IN**	1B: 4,6, 8,10	BUS GRANT (0-3) IN: Totem-pole driven signals generated by the Arbiter or Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant In signal indicates to this board that it may become the next bus master.
BG0OUT*-BG3OUT*	1B: 5,7, 9,11	BUS GRANT (0-3) OUT: Totem-pole driven signals generated by Requesters. Bus Grant In and Out signals form a daisy-chained bus grant. The Bus Grant Out signal indicates to the next board that it may become the next bus master.
BR0*-BR3*	1B: 12-15	BUS REQUEST (0-3): Open-collector driven signals generated by Requesters. These signals indicate that a DTB master in the daisy-chain requires access to the bus.
DS0*	1A: 13	DATA STROBE 0: Three-state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D00-D07).
DS1*	1A: 12	DATA STROBE 1: Three state driven signal that indicates during byte and word transfers that a data transfer will occur on data bus lines (D08-D15).

Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
DTACK*	1A: 16	DATA TRANSFER ACKNOWLEDGE: Open-collector driven signal generated by a DTB slave. The falling edge of this signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
D00-D15	1A: 1-8 1C: 1-8	DATA BUS (bits 0-15): Three-state driven bi-directional data lines that provide a data path between the DTB master and slave.
GND	1A: 9,11, 15,17,19 1B: 20,23 1C: 9 2B: 2,12 22,31	GROUND
IACK*	1A: 20	INTERRUPT ACKNOWLEDGE: Open-collector or three-state driven signal from any Master processing an interrupt request. It is routed via the backplane to Slot 1, where it is looped back to become Slot 1 IACKIN* to start the interrupt acknowledge daisy-chain.
IRQ1*- IRQ7*	1B: 24-30	INTERRUPT REQUEST (1-7): Open-collector driven signals, generated by an interrupter, which carry prioritized interrupt requests. Level seven is the highest priority.
LWORD*	1C: 13	LONGWORD: Three-state driven signal to indicate that the current transfer is a 32-bit transfer.
(RESERVED)	2B: 3	RESERVED: Signal line reserved for future VMEbus enhancements. This line must not be used.
SERCLK	1B: 21	A reserved signal which will be used as the clock for a serial communication bus protocol which is still being finalized.
SERDAT	1B: 22	A reserved signal which will be used as the transmission line for serial communication bus messages.

Table B-1. VMEbus Signal Identification (cont'd)

Signal Mnemonic	Connector and Pin Number	Signal Name and Description
SYSCLK	1A: 10	SYSTEM CLOCK: A constant 16-MHz clock signal that is independent of processor speed or timing. It is used for general system timing use.
SYSFAIL*	1C: 10	SYSTEM FAIL: Open-collector driven signal that indicates that a failure has occurred in the system. It may be generated by any module on the VMEbus.
SYSRESET*	1C: 12	SYSTEM RESET: Open-collector driven signal which, when low, will cause the system to be reset.
WRITE*	1A: 14	WRITE: Three-state driven signal that specifies the data transfer cycle in progress to be either read or written. A high level indicates a read operation; a low level indicates a write operation.
+5V STDBY	1B: 31	+5 Vdc STANDBY: This line supplies +5 Vdc to devices requiring battery backup.
+5V	1A: 32 1B: 32 1C: 32 2B: 1,13,32	+5 Vdc Power: Used by system logic circuits.
+12V	1C: 31	+12 Vdc Power: Used by system logic circuits.
-12V	1A: 31	-12 Vdc Power: Used by system logic circuits.

BACKPLANE CONNECTOR P1

The following table lists the P1 pin assignments by pin number order. (The connector consists of three rows of pins labeled rows A, B, and C.)

Table B-2. P1 Pin Assignments

Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GDN
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK (1)	A17
22	IACKOUT*	SERDAT (1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

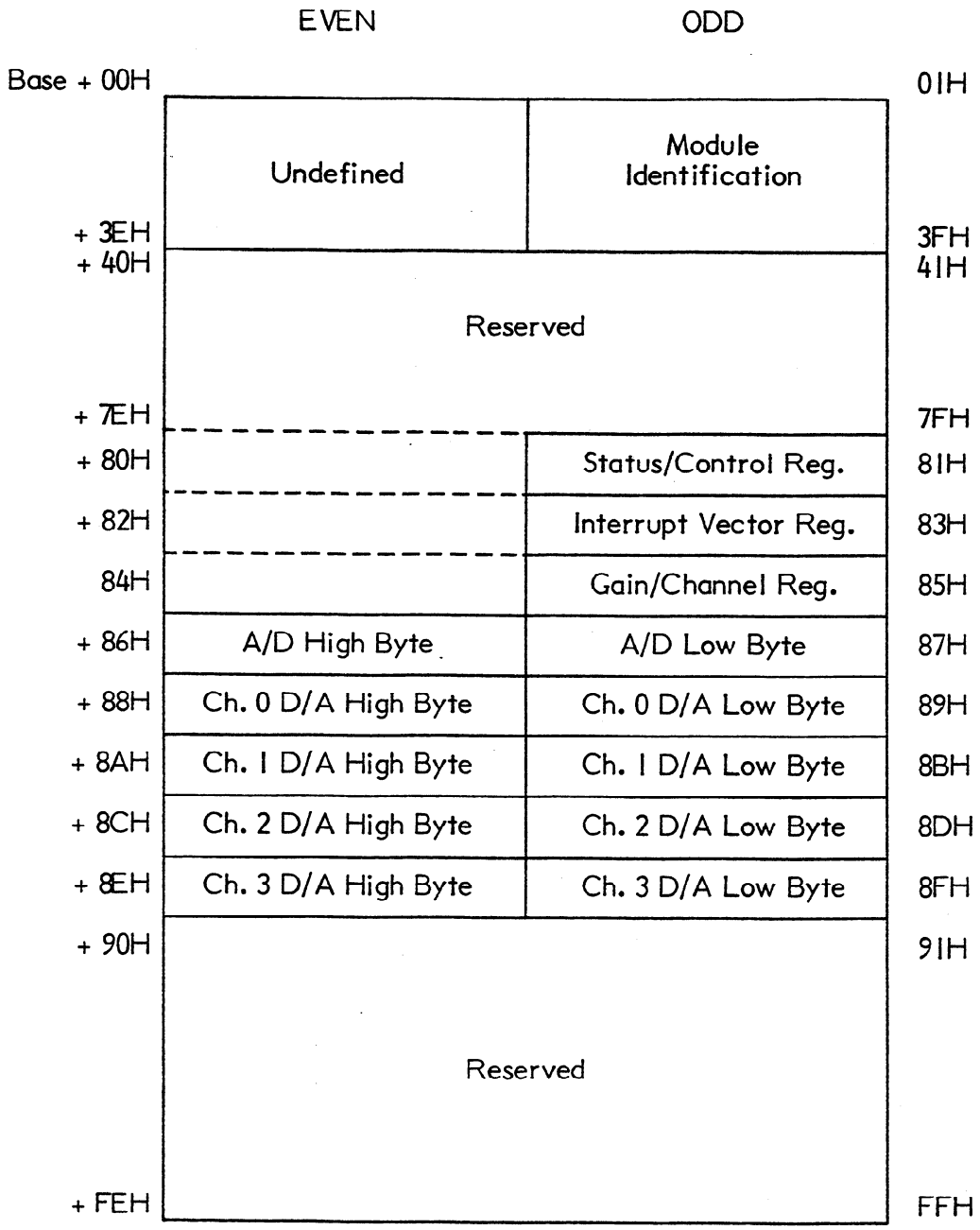
Table B-3. P2 - Power and Ground Signals

Signal Mnemonic	Connector and Pin Number	Signal Name
GND	2B:2 2B:12 2B:22 2B:31	Ground
+5V	2B:1 2B:13 2B:32	+5Vdc Power used by the system logic circuits

Appendix D

QUICK REFERENCE GUIDE

AIO Module Memory Map



AIO Module Jumpers/Switches

VMEbus Options	
Switch Bank S1	Use
Switches 1-6	Module base address select (refer to Section 2.5.1).
Switch 7	This switch determines whether the module will respond to only supervisory accesses or to both supervisory and non-privileged accesses (refer to Section 2.5.3).
Switch 8	This switch works in conjunction with jumper J2 to determine whether the board operates with address modifiers for the short I/O address space or those for the standard address space (refer to Section 2.5.2).
Switch Bank S2	Use
Switches 1-3	Interrupt level select for any interrupts generated by the module (refer to Section 2.5.5).
Jumpers	Use
J1	Selects either the use of on-board IACK* arbitration or the routing of the IACKIN* signal directly to the IACKOUT* signal, at the P1 connector. This jumper works in conjunction with jumper J3. If jumper J3 is not set to enable on-board IACK* arbitration, the daisy-chain will not be complete (refer to Section 2.5.6).
J2	This jumper works in conjunction with switch bank S1 (switch 8) for address space selection (i.e., short I/O address space or standard address space). (Refer to Section 2.5.2.)
J3	This jumper either enables or disables the on-board IACK* arbitration circuitry. The on-board arbitration must be enabled if the board is to be a part of IACK* daisy-chain (refer to Section 2.5.6).

Digital to Analog Conversion Options

Jumpers	Use
J8	This jumper will automatically set the D/A data lines to either all logic "1's" or all logic "0's" during system reset or power-up (refer to Section 2.6.1).
J12-J15	These jumpers provide the option to individually configure the output channels to convert either straight binary to analog or to convert two's complement binary to analog (refer to Section 2.6.2).
(J23,J24,J25,J26) (J27,J28,J29,J30) (J31,J32,J33,J34) (J35,J36,J37,J38)	These groups of jumpers select one of five output voltage ranges for each output channel. Four of these jumpers also activate calibration potentiometers (specific to each channel) to provide for the adjustment of either unipolar voltage offset or for the adjustment of bipolar voltage offset (refer to Section 2.6.4).
J39-J42	These jumpers configure the four output channels to convert data to either an analog voltage format or an analog current format (refer to Section 2.6.3).

Analog to Digital Conversion Options

Jumpers	Use
J9 and J10	These jumpers provide the option of converting analog inputs to either a two's complement format or to a straight/offset binary format (refer to Section 2.7.1).
J16,J20, and J43	These jumpers are all used together to determine if the inputs will be configured as 16 differential or as 32 single-ended lines (refer to Section 2.7.2).
J17 and J21	These jumpers are used to configure the inputs for either bipolar or unipolar input voltages (refer to Section 2.7.3).
J18	This jumper configures the input voltage range for 0-5V and ±2.5V inputs (refer to Section 2.7.3).
J19	This jumper selects the 0-10V input range (refer to Section 2.7.3).
J22(cluster)	This jumper configuration selects one of three input stage gain ranges for the input channels (refer to Section 2.7.4).
J44 and J45	These two jumpers are provided to allow grounding of an input channel in either the single-ended or the differential input mode of operation for purposes of calibration (refer to Section 2.7.5).

Base Address Switch Options

Addressing Options

Jumper	Switch 8 (S1)	Option Selected
J2A	Open	Standard Data Access Operation
J2B	Closed	Short I/O Access Operation

Connector Pin-Outs

Input Connector JK1

JK1

Pin	Single-ended Configuration	Differential Configuration
1	Channel 0	Channel 0 Lo
2	Channel 8	Channel 0 Hi
3	Analog Ground	Analog Ground
4	Channel 9	Channel 1 Hi
5	Channel 1	Channel 1 Lo
6	Analog Ground	Analog Ground
7	Channel 2	Channel 2 Lo
8	Channel 10	Channel 2 Hi
9	Analog Ground	Analog Ground
10	Channel 11	Channel 3 Hi
11	Channel 3	Channel 3 Lo
12	Analog Ground	Analog Ground
13	Channel 4	Channel 4 Lo
14	Channel 12	Channel 4 Hi
15	Analog Ground	Analog Ground
16	Channel 13	Channel 5 Hi
17	Channel 5	Channel 5 Lo
18	Analog Ground	Analog Ground
19	Channel 6	Channel 6 Lo
20	Channel 14	Channel 6 Hi
21	Analog Ground	Analog Ground
22	Channel 15	Channel 7 Hi
23	Channel 7	Channel 7 Lo
24	Analog Ground	Analog Ground
25	Channel 16	Channel 8 Lo
26	Channel 24	Channel 8 Hi
27	Analog Ground	Analog Ground
28	Channel 25	Channel 9 Hi
29	Channel 17	Channel 9 Lo
30	Analog Ground	Analog Ground
31	Channel 18	Channel 10 Lo
32	Channel 26	Channel 10 Hi

Input Connector JK1 (continued)

JK1

Pin	Single-ended Configuration	Differential Configuration
33	Analog Ground	Analog Ground
34	Channel 27	Channel 11 Hi
35	Channel 19	Channel 11 Lo
36	Analog Ground	Analog Ground
37	Channel 20	Channel 12 Lo
38	Channel 28	Channel 12 Hi
39	Analog Ground	Analog Ground
40	Channel 29	Channel 13 Hi
41	Channel 21	Channel 13 Lo
42	Analog Ground	Analog Ground
43	Channel 22	Channel 14 Lo
44	Channel 30	Channel 14 Hi
45	Analog Ground	Analog Ground
46	Channel 31	Channel 15 Hi
47	Channel 23	Channel 15 Lo
48	Analog Ground	Analog Ground
49	Power Ground	Power Ground
50	External Trigger	External Trigger

Input Connector JK2

JK2

Pin	Pin Description
1	Channel 0 Vout
2	NC
3	Analog Ground
4	NC
5	Channel 1 Vout
6	Analog Ground
7	Channel 2 Vout
8	NC
9	Analog Ground
10	NC
11	Channel 3 Vout
12	Analog Ground
13	NC
14	NC
15	Analog Ground
16	NC
17	NC
18	Analog Ground
19	NC
20	NC

Input Connector JK2 (continued)

JK2

Pin	Pin Description
21	Analog Ground
22	NC
23	NC
24	Analog Ground
25	NC
26	NC
27	Channel 0 Iout+
28	Iout-
29	Iout-
30	Channel 1 Iout+
31	Channel 2 Iout+
32	Iout-
33	Iout-
34	Channel 3 Iout+

Module Base Address List

Switches						VME base address in VME Short I/O Address space
6(A15)	5(A14)	4(A13)	3(A12)	2(A11)	1(A10)	
0	0	0	0	0	0	0000H
0	0	0	0	0	1	0400H
0	0	0	0	1	0	0800H
0	0	0	0	1	1	0C00H
0	0	0	1	0	0	1000H
0	0	0	1	0	1	1400H
0	0	0	1	1	0	1800H
0	0	0	1	1	1	1C00H
0	0	1	0	0	0	2000H
0	0	1	0	0	1	2400H
0	0	1	0	1	0	2800H
0	0	1	0	1	1	2C00H
0	0	1	1	0	0	3000H
0	0	1	1	0	1	3400H
0	0	1	1	1	0	3800H
0	0	1	1	1	1	3C00H
0	1	0	0	0	0	4000H
0	1	0	0	0	1	4400H
0	1	0	0	1	0	4800H
0	1	0	0	1	1	4C00H
0	1	0	1	0	0	5000H
0	1	0	1	0	1	5400H
0	1	0	1	1	0	5800H
0	1	0	1	1	1	5C00H
0	1	1	0	0	0	6000H
0	1	1	0	0	1	6400H
0	1	1	0	1	0	6800H
0	1	1	0	1	1	6C00H
0	1	1	1	0	0	7000H
0	1	1	1	0	1	7400H
0	1	1	1	1	0	7800H
0	1	1	1	1	1	7C00H
1	0	0	0	0	0	8000H
1	0	0	0	0	1	8400H
1	0	0	0	1	0	8800H
1	0	0	0	1	1	8C00H
1	0	0	1	0	0	9000H
1	0	0	1	0	1	9400H
1	0	0	1	1	0	9800H
1	0	0	1	1	1	9C00H
1	0	1	0	0	0	A000H
1	0	1	0	0	1	A400H
1	0	1	0	1	0	A800H
1	0	1	0	1	1	AC00H
1	0	1	1	0	0	B000H
1	0	1	1	0	1	B400H
1	0	1	1	1	0	B800H
1	0	1	1	1	1	BC00H
1	1	0	0	0	0	C000H
1	1	0	0	0	1	C400H
1	1	0	0	1	0	C800H
1	1	0	0	1	1	CC00H
1	1	0	1	0	0	D000H
1	1	0	1	0	1	D400H
1	1	0	1	1	0	D800H
1	1	0	1	1	1	DC00H
1	1	1	0	0	0	E000H
1	1	1	0	0	1	E400H
1	1	1	0	1	0	E800H
1	1	1	0	1	1	EC00H
1	1	1	1	0	0	F000H
1	1	1	1	0	1	F400H
1	1	1	1	1	0	F800H
1	1	1	1	1	1	FC00H

NOTE Open = Logic "1"
Closed = Logic "0"