DAC128V

8-Channel, 12-bit, 8-range
±10 V Digital-to-Analog Board
Hardware Reference

Document No. B-T-MR-DAC128V#-A-0-A4

FOREWORD

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FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1. INTRODUCTION

1.1 How to Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 8-channel, 12-bit, 8-range ±V Digital to Analog Converter (DAC) IndustryPack (also called IP Module) board, referred to in this manual as the DAC128V (part number BHAS-DAC128V).

1.1.2 Scope

This reference manual covers the physical and operational description of the DAC128V, both from hardware and software perspectives. This manual also contains detailed technical information about the DAC128V's performance characteristics, and some typical applications.

You need a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of the use of IP Modules on a carrier board to effectively use this manual.

1.1.3 Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Bus Onboard the Motorola MVME162 Controller* (Doc. A-T-ST-IPAC2001)
- *American National Standard for IP Modules (ANSI/VITA 4 - 1995)* published by VMEbus International Trade Association (VITA), 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA. Phone: 480-951-8866, FAX: 480-951-0720, E-mail: info@vita.com, URL: www.vita.com

- Systran Corporation: www.systran.com

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Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

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2. PRODUCT OVERVIEW

2.1 Overview

The DAC128V is a singlewide IP Module board, conforming both mechanically and electrically to the ANSI VITA/4-1995, *American National Standard for IP Modules*. For a typical IP Module carrier that holds four IP Modules, it can provide up to 32 channels of DACs for a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution.

The DAC128V maintains the highest possible accuracy by minimizing accumulative errors through the use of the best parts for the tasks to be accomplished.

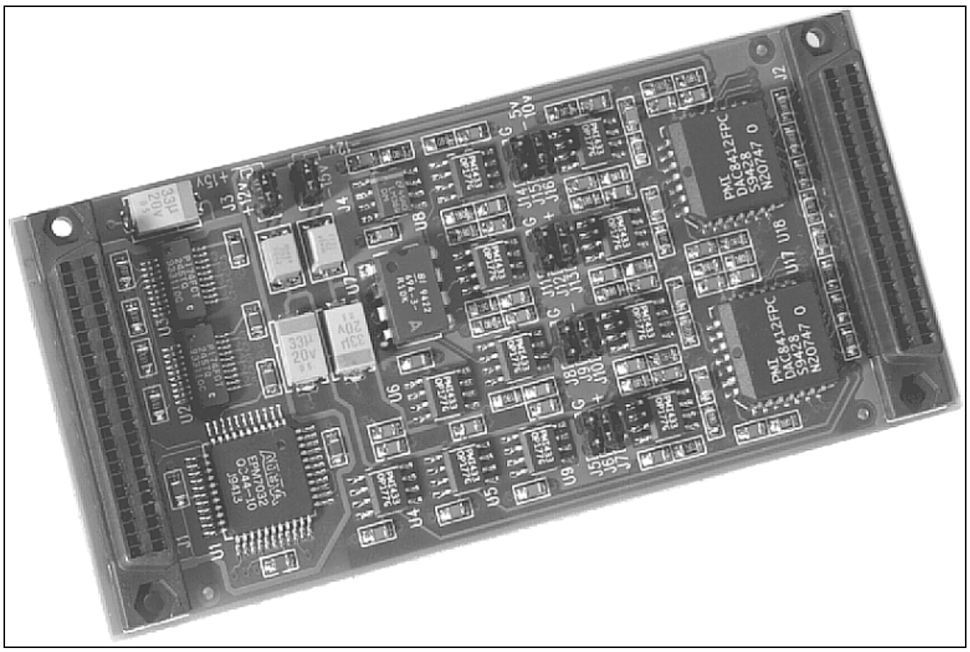

Figure 2-1 DAC128V Board

2.2 Features

- Eight independent channels of 12-bit resolution DACs in two groups of four outputs scaled to one of eight possible voltage ranges between ±10 V, with no-wait write and read-back accesses
- Jumper selectable output voltage ranges: 0 ⇒ +5 V, 0 ⇒ +10 V, -5 ⇒ 0 V, -5 ⇒ +5 V, -5 ⇒ +10 V, -10 ⇒ 0 V, -10 ⇒ +5 V, -10 ⇒ +10 V
- Output current is ±20 mA (Max.) for ±10 V output (running on ±15 V power)
- Buffered reference outputs: -10 V, -5 V, +5 V, and +10 V
- Jumper selectable analog power sources: ±12 V from carrier, or ±15 V from I/O connector (recommended for 10 V ranges)
- Integral and differential nonlinearities are ±1 LSB (Max.); settling time is 6 µs (Typical); Slew rate of 2.2 V/µs (Typical)

- $Vout = Vref\_{low} + \frac{(Vref\_{high} - Vref\_{low}) * N}{4096}$ (where N = decimal digital code)
- Straight binary coding; DAC output at Mid-scale on power-up.

2.3 Related Products

- Software: 'C' library and OS-9 device driver routines with documentation.

2.4 Block Diagram Description

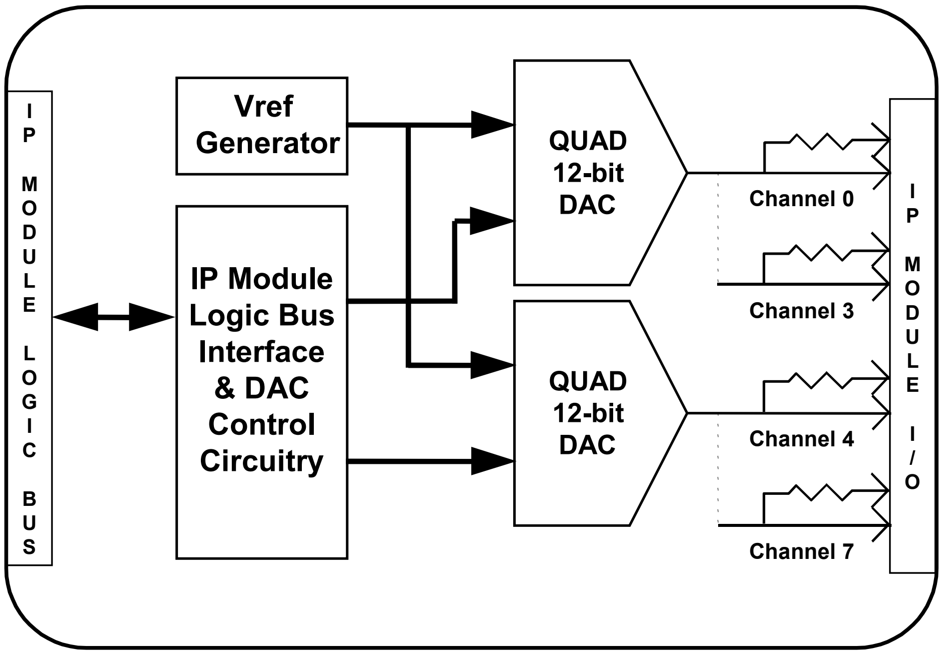

Figure 2-2 DAC128V Simplified Block Diagram

Figure 2-2 presents a simplified block diagram of the DAC128V. On the left side is the IP Module's Logic Bus connector through which all transfers between the IP Module carrier and the DAC128V's registers and data sources are conducted. The block labeled "IP Module Logic Bus Interface and DAC Control Circuitry" contains the ID "PROM" data, the DACs' access detection and control logic, the IP Module transfer sequence/control logic, and the data path gate control signals. All of this circuitry is implemented in one small EPLD. The block labeled "Vref Generator" consists of a precision (+10.000) voltage reference, a quad voltage (±10 V, ±5 V) derivation circuit with buffers, two sets of high and low reference voltage selection blocks with buffers (one set per quad DAC), and four reference voltage buffers with connections to the I/O connector (not shown in this block diagram).

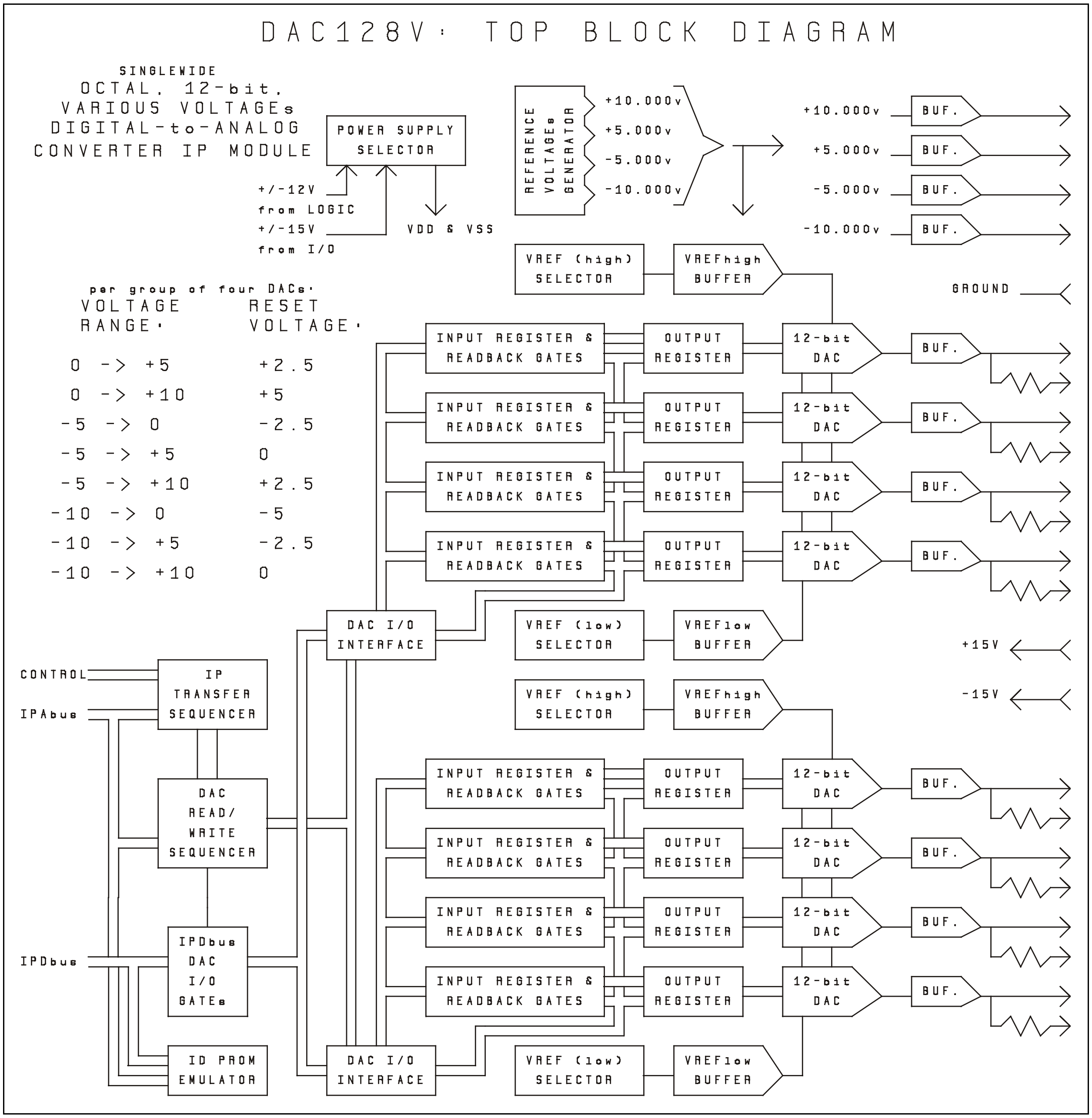

Figure 2-3 Detailed Block Diagram

Each of the elements labeled “QUAD 12-bit DAC” consists of four 12-bit digital-to-analog converters with output voltage buffers, individual high and low reference inputs shared by all four DACs, double-buffered WRITE registers, and read-back gating. As depicted in Figure 2-2, all eight DAC outputs have both direct connections, and series-resistance connections (for applications with highly capacitive loads) to the I/O connector. On the right side is the DAC128V’s I/O connector, providing sixteen DAC analog outputs, four buffered reference outputs, two external power supply inputs, and 28 connections to the ground plane.

Figure 2-3 presents a detailed block diagram of the DAC128V. Again, on the left side is carrier ↔ IP Module interface via the IPDbus, the IPAbus, and the access Control signals. The block labeled "IPDbus DAC I/O GATEs" consists of a pair of bi-directional bus transceivers for buffering the writes and quickly terminating read operations.

This second level "top" block diagram provides more detail to better understand the inner functional elements of each of the quad DAC units, including the digital registration and read-back capabilities, the buffered high and low voltage references, and the buffered outputs to the I/O connector. Also provided in more detail (at the top of Figure 2-3) is the ability to run this board using external (clean) power supplies, and the quad-reference voltage generator, with individual buffers for the reference outputs to the I/O connector.

The table on the (upper half) left side of Figure 2-3 provides all of the eight valid voltage ranges that can be selected per quad DAC unit, and their respective (centered) power-up default voltage outputs.

2.5 Detailed Description

The DAC128V was developed using VHDL and Synthesis, targeted to an Altera EPLD, schematic captured and integrated to standard integrated circuits, connectors, and discrete components using VIEWLogic's ViewDraw and associated packages.

2.6 Digital Components and their Functions

All IP Module Logic Bus transfers take place across J1, the IP Module Logic Connector, located on the left side of all block diagrams. Refer to the *ANSI/VITA 4-1995* specifications for details about the signals on this connector. This IP Module does not support DMA or Interrupts, and has no memory accesses.

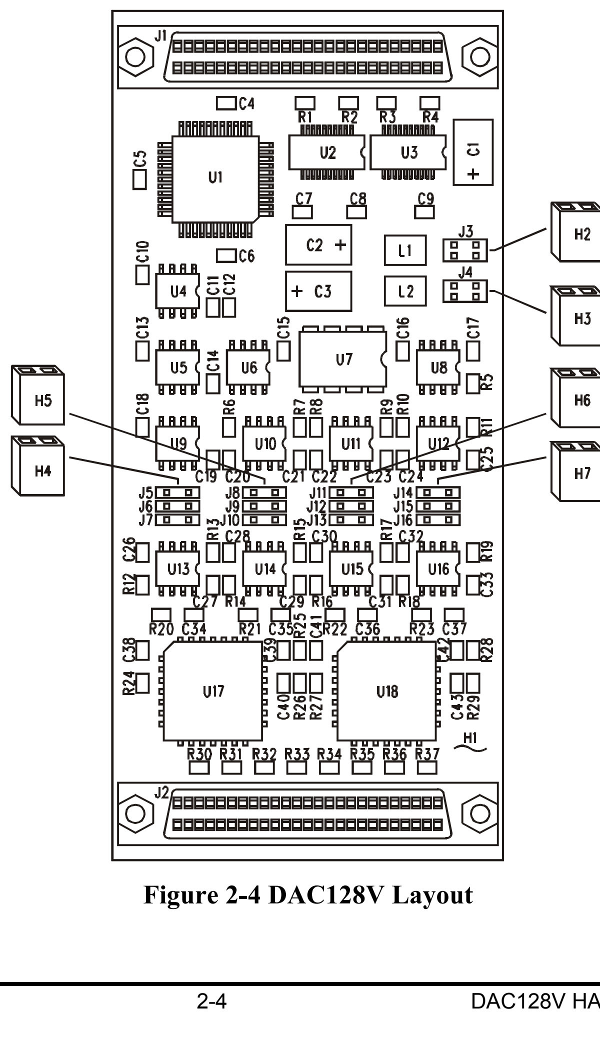

Figure 2-4 DAC128V Layout

It performs no-wait ID reads, and no-wait reads from and writes to a short, eight-location I/O map. Figure 2-4 is a physical assembly drawing for the DAC128V. Connector J1 is located at the top of this drawing.

The DAC128V's primary activity controller "S_DA128V" is housed within the EPM7032LC44-10 EPLD located at U1 (just below J1 in Figure 2-4). It serves as the IP Module transfer engine, whose responsibilities include:

- Detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier.
- ID PROM emulation data pattern generation for ID read transfers.
- DAC chip select and read/write control signal generation for I/O reads and (16-bit only) writes where QDAC#1 at U17 is enabled for the first four I/O locations and QDAC#2 at U18 is enabled for the last four I/O locations.
- Direction with output-enable control signals for the data bus coupling (IPDbus ↔ DACDbus) transceivers.

The data bus transceivers are implemented using a pair of 74FCT245SC devices, and are designated U2 and U3 (just below J1 to the right of U1 in Figure 2-4). Normally an IP Module does not require data bus transceivers. However, since the DACs' specified time for release of the data bus during read operations (low impedance ⟶ high impedance state change time) exceeds the maximum time allowed by the ANSI/VITA 4-1995 specification, these transceivers are employed to quickly decouple the data buses.

2.7 DAC's Voltage Ranges

The following description provides the user with the information necessary to properly set the voltage output ranges for the DACs on the DAC128V. In general, there are three high-side reference voltage levels and three low-side reference voltage levels per group of four DAC outputs. There is one combination that is not logical for normal operations, and this is the default shipment state of the DAC128V.

CAUTION: The DAC's produce an invalid output when both high and low references are set to ground; the voltage outputs remain at 0.000 V (±1.0 mV) regardless of the binary code written to their respective registers.

This "shipped-state" configuration requires the user carefully ascertain and set the output voltage ranges prior to using the DAC128V. The intent in shipping the DAC128V in this benign state is to attempt to minimize the potential impact on the user's external circuitry to which the DAC128V is attached if it is simply installed upon arrival without properly configuring the voltage range selections. Refer to the assembly drawing in Figure 2-4 for the following four topic areas.

2.7.1 High Reference For QDAC#1

The high-side reference for the first four DAC outputs generated by QDAC#1 at U17 is selected by placing the jumper shunt designated as H4 onto one pair of three jumper pads designated as J5 (ground or 0.000 V), J6 (+5.000 V), or J7 (+10.000 V). The selection is buffered by the Operational Amplifier at U13, which provides the high-side reference voltage for QDAC#1. Using J6 or J7 is valid for any configuration. Use of J5 should occur if, and only if, J8 is not used for the low reference for QDAC#1 (see subsection 2.7.2, below).

2.7.2 Low Reference For QDAC#1

The low-side reference for the first four DAC outputs generated by QDAC#1 at U17 is selected by placing the jumper shunt designated as H5 onto one pair of the three jumper pads designated as J8 (ground or 0.000 V), J9 (-5.000 V), or J10 (-10.000 V). The Operational Amplifier at U14 buffers the selection, which provides the low-side reference voltage for QDAC#1. Using J9 or J10 is valid for any configuration. Use of J8 should occur if, and only if, J5 is not used for the high reference for QDAC#1 (see subsection 2.7.1, above).

2.7.3 High Reference For QDAC#2

The high-side reference for the last four DAC outputs generated by QDAC#2 at U18 is selected by placing the jumper shunt designated as H6 onto one pair of three jumper pads designated as J11 (ground or 0.000 V), J12 (+5.000 V), or J13 (+10.000 V). The Operational Amplifier at U15 buffers the selection, which in turn provides the high-side reference voltage for QDAC#2. Using J12 or J13 is valid for any configuration. Use of J11 should occur if, and only if, J14 is not used for the low reference for QDAC#2 (see 2.7.4, below).

2.7.4 Low Reference For QDAC#2

The low-side reference for the last four DAC outputs generated by QDAC#2 at U18 is selected by placing the jumper shunt designated as H7 onto one pair of the three jumper pads designated as J14 (ground or 0.000 V), J15 (-5.000 V), or J16 (-10.000 V). The Operational Amplifier at U16 buffers the selection, which provides the low-side reference voltage for QDAC#2. Using J15 or J16 is valid for any configuration. Use of J14 should occur if, and only if, J11 is not used for the high reference for QDAC#2 (see 2.7.3, above).

2.8 Reference Voltage Generation

The principle voltage reference is the LM369DM device at U8, and is based upon a buried zener reference technology. Its nominal output voltage is +10.000 V, with a typical error of ±70 ppm or ±700 µV. Its temperature coefficient over the product's specified operating range is typically 5 ppm/°C. The multi-reference generator places a constant load on this voltage reference, regardless of the demands of the DACs or the user’s loads for the reference voltages supplied to the I/O connector. That load is a constant 500 µA. The 0.1 µF capacitor at C16 provides additional noise filtering such that the noise voltage is reduced to a typical value of 4 µVrms for the spectrum of 10 Hz through 10 kHz.

This reference has a relatively low drop-out voltage ceiling which enables proper operation even when running the DAC128V from a carrier-sourced ±12 V supply. At 25°C, the minimum supply voltage is about +11 V, with it increasing to about +11.5 V for the low temperature operations of the DAC128V, and down to about +10.5 V for the high temperature end. The reference generator’s power supply connections are identical to those of the remaining analog circuitry, and are switched to the externally supplied power sources when jumpered to do so (see section 2.9, below).

The resistor divider network located at U7, in conjunction with the three Operational Amplifiers at U10, U11, and U12 derive the remaining three reference voltages (not supplied by U8): +5.000 V, -5.000 V, and -10.000 V. U7 contains four 10 KΩ resistors that have an absolute tolerance (not very important for this application) of ±0.1%, and a ratiometric tolerance of ±0.05% (very important) that track at 5 ppm/°C, in the worst case.

All four reference voltages are buffered by the four Operational Amplifiers at U4, U5, U6, and U9 to provide the user with outputs at the I/O connector for the voltages of +10.00 V, -5.00 V, +5.00 V, and -10.00 V, respectively.

2.9 External Analog Supply

The DAC128V has provisions for running all of its analog circuitry off of an external power source. There are at least two reasons for taking this action. First, some applications may require "quieter" performance than is possible using the carrier's power sources. These are usually developed using noisier "switcher" technology than the older "linear" techniques.

Second, and more importantly, the external power source provides greater accuracy. While the reference circuitry is capable of running well from the +12 V provided by a carrier, the DAC128V will not be able to maintain accuracy specifications when using either of the +10 V rails to drive loads.

The DAC128V is shipped with the analog power selections configured for running from the carrier's ±12 V supplies. This is implemented by the placement of the shunt H2 at the two-by-two jumper block designated J3, and the shunt H3 at the jumper block J4 at the top (towards the IP Module logic connector J1, away from the I/O connector J2) pair of jumper pins. The printed circuit board's silk-screen has these positions labeled as "+12v" and "-12v", respectively.

To operate the DAC128V from external (±12 →) ±15 V supplies:

- First ensure that the +15 V is wired to pin 48 of the I/O connector, and that -15 V is wired to pin 45 of the I/O connector.
- Ensure its power supply ground is well connected to the DAC128V's ground connections at J2.
- Then, move jumper H2 to the bottom connections of J3, and move jumper H3 to the bottom connections of J4 (bottom ≡ away from the logic connector J1, towards the I/O connector J2).

These positions are silk-screen labeled on the printed circuit board as "+15v" and "-15v", respectively.

2.10 The Buffers

There are eleven analog buffers used on the DAC128V, located at U4, U5, U6, U9, U10, U11, U12, U13, U14, U15, and U16. They are all configured as unity-gain (non-inverting) voltage followers, all using the ultra-precision Operational Amplifier #OP177GS. This device was selected because it provides performance characteristics that approach those typically only possible with chopper-stabilized amplifiers, without the usual "chopper" problems of noise and spikes, large size with mandatory external storage capacitors, limited common-mode input ranges, and high expense.

The 60 µV maximum input offset voltage (over temperature) is so small that offset voltage reduction circuitry implemented with trim-potentiometers would fail to provide significant accuracy improvements over temperature due to the tracking problems of dissimilar temperature coefficients between the Operational Amplifiers and the potentiometers. Therefore, all buffers are untrimmed, which also increases reliability and reduces costs.

2.11 The DACs

Most of the functional and architectural topics concerning the DACs used have been covered. For the sake of completeness, both DACs are supplied by Analog Devices, #DAC-8412FPC.

NOTE: This technology was obtained from the former company "PMI" and that these two devices, designated as U17 and U18, may be marked as PMI instead of AD or ADI.

The technical specifications in Appendix A, and the performance data presented in Chapter 4 completely cover the remaining text concerning the DACs. Comparison of the specifications published as tables by Analog Devices and to those presented in this document will reveal certain anomalies. The specifications presented in Appendix A include (beyond those of ADI) empirical data as well as information obtained from characteristic curves, and not just those tabulated by ADI.

2.12 DAC128V Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents are safe to use that are based on: Fluorine, Chlorine, Aqueous, and Alcohol.

CAUTION: Do NOT use gasoline or thinner-type solvents on this product.

3. INSTALLATION

3.1 Unpack the DAC128V

The contents of the DAC128V shipping package is listed in Table 3-1:

Table 3-1 Contents of DAC128V Shipping Package

Qty	Description
1	DAC128V Printed Circuit Assembly
1	DAC128V Hardware Reference Manual *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

*	One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g., BTMR-DAC128V).

3.2 Visually Inspect the DAC128V

Examine the DAC128V to determine if any damage occurred during shipping.

3.3 Install the DAC128V

NOTE: The DAC128V is an Electrostatic Sensitive Device (ESD). Install the DAC128V on an anti-static workbench using good ESD practices to protect the IP Module and its host carrier board.

The DAC128V installation requires the following tools:

Table 3-2 DAC128V Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

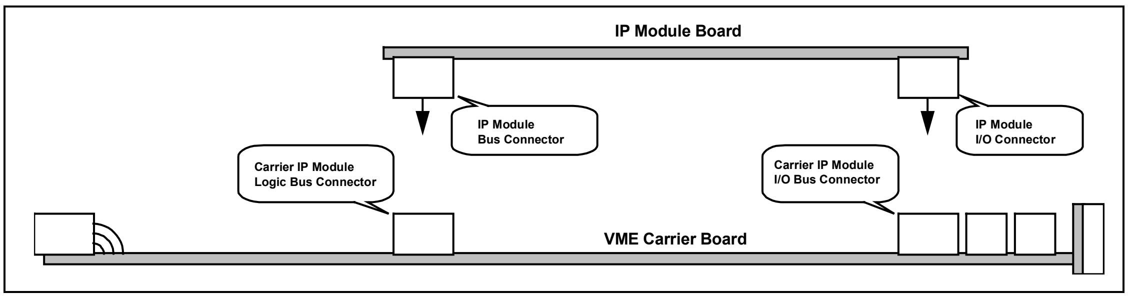

Figure 3-1 Installation of the DAC128V on a VME IP Module Carrier Board

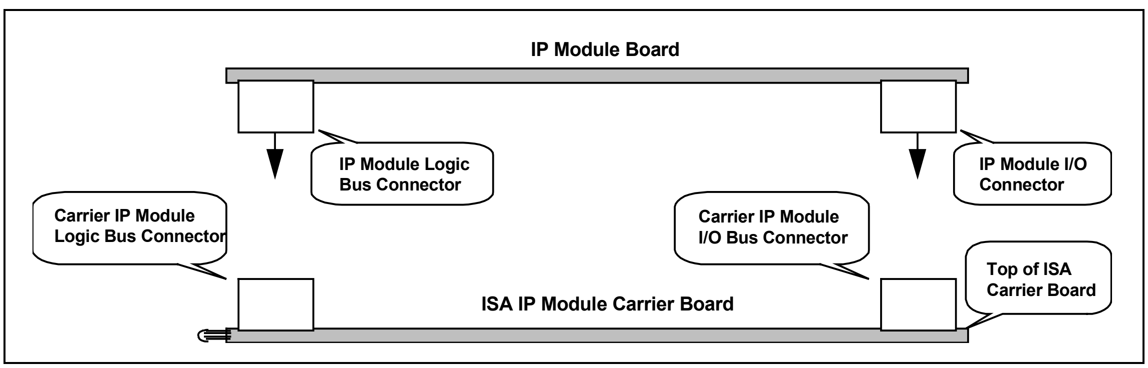

Figure 3-2 Installation of the DAC128V on an ISA IP Module Carrier Board.

Figure 3-1 shows how the DAC128V is installed on a VME IP Module carrier, and Figure 3-2 shows the installation on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module carrier board hardware reference manual for more information.

Referring to the appropriate figures and tables described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the DAC128V can be made.
3. Remove the DAC128V from the shipping package and place it on the ESD bench.
4. Install the DAC128V onto the carrier board by applying adequate and equal pressure to the DAC128V board at both ends.

*5. Install four M2x5 mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the DAC128V to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	GND
48	+15VIN
47	GND
46	GND
45	-15VIN
44	GND
43	GND
42	-10VOUT
41	GND
40	GND
39	-5VOUT
38	GND
37	GND
36	+5VOUT
35	GND
34	GND
33	+10VOUT
32	GND
31	GND
30	GND
29	GND
28	GND
27	GND
26	GND
25	2DAC08R
24	DAC08
23	GND
22	2DAC07R
21	DAC07
20	GND
19	2DAC06R
18	DAC06
17	GND
16	2DAC05R
15	DAC05
14	GND
13	2DAC04R
12	DAC04
11	GND
10	2DAC03R
9	DAC03
8	GND
7	2DAC02R
6	DAC02
5	GND
4	2DAC01R
3	DAC01
2	GND
1	GND

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4. PERFORMANCE

4.1 Overview

The purpose of this section is to provide several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Appendix A, SPECIFICATIONS. Where possible, data is tabulated with only one response time (actual) performance figure presented in order to minimize the length of the presentation.

4.2 Timing measurements

Timing measurements were conducted on the DAC128V using an HP model 16500A Logic Analyzer with a 400 megasamples per second Digitizing Oscilloscope Module, model 16531A, plugged into slot E, and a 1 GHz Timing Master Module, model 16515A in slot C. The DAC128V was installed in the IP Module slot ‘A’ of a Motorola MVME-162-01 VME processor IP Module carrier board. Figure 4-1 shows the test configuration for the oscilloscope and state timing measurements.

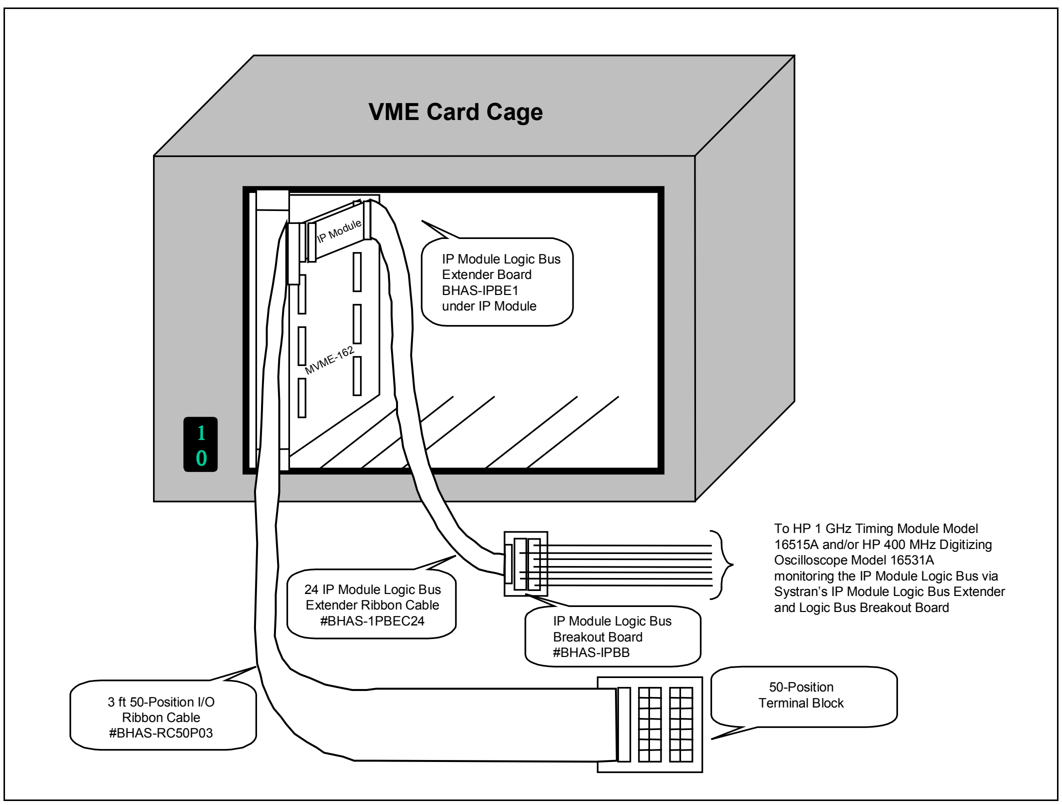

Figure 4-1 IP Module Test Configuration for Oscilloscope and State Timing Measurements

4.3 IP Module Accesses

There are some parameters that are important when evaluating an IP Module's performance on a specific carrier board. These involve the assertion and negation, or driving to logic state versus high impedance states, of signals from the IP Module to the carrier, with reference to the rising edge of ICLK. According to specification, these state changes must occur within 40 ns. Figure 4-2 presents just one of the logic state analysis figures captured for the development of the data in Table 4-1. Table 4-2 depicts an I/O write to the first I/O location (IPA = 0x00) of data whose least significant nibble is zero (IPD[3:0] = 0). The important parameter here is that it typically takes 10 ns to negate N_ACK.

Table 4-1 IP Module Access Time

Function/Operation	ICLK Until	Time
I/O READ @ IPA = 0x00	N_ACK	10 ns
I/O READ @ IPA = 0x00	N_ACK	11 ns
I/O READ @ IPA = 0x00	IPDbus' HIGH to LOW impedance	22 ns
I/O WRITE @ IPA = 0x00	N_ACK	09 ns
I/O WRITE @ IPA = 0x00	N_ACK	10 ns
ID READ @ IPA = 0x00	IPDbus' HIGH to LOW impedance	06 ns
ID READ @ IPA = 0x00	N_ACK	10 ns
ID READ @ IPA = 0x00	N_ACK	11 ns

There is one additional note to add concerning DAC128V IP Module operations. Normally, an IP Module does not drive the IPDbus to a low impedance state until (and during) its assertion of N_ACK during HOLD and termination cycles. To date, this policy has been faithfully followed in the design of all Systran's IP Modules. The best practical reason for this is to avoid data bus contention with a carrier or other IP Module that is slow to release the IPDbus following a preceding transfer without an idle cycle. The specification requires the release within 40 ns. There is no restriction against an IP Module driving the IPDbus during the select cycle.

The DAC's read-back registers have a very long data valid delay time, potentially approaching 160 ns following the assertion of their appropriate chip-select signal. For this reason, the IPDbus is coupled to the DAC's read buffers as soon as possible in the read transfer to provide the maximum amount of time for data line stabilization and carrier data setup time for capturing the data in the rising edge of the ICLK signal at the termination of the transfer. This phenomenon is depicted in Figure 4-2, and Figure 4-3. Figure 4-3 also shows why READ gates were installed, as described in Chapter 2, PRODUCT OVERVIEW.

4.4 Wrong Supply Impact

It is important to use the provisions of external analog power source when attempting to use any of the eight analog voltage ranges that include either or both +10.0 V and -10.0 V outputs. By specification, the supply voltage must be a minimum of ±12.5 V, with ±15 V recommended; especially for heavy loads (see paragraph 4.3 and 4.4). When this rule is violated, the results are undetermined.

Table 4-2 presents some data that is typical of the problem that may result. If you are not getting smooth changes in output for even code changes, this could be the reason.

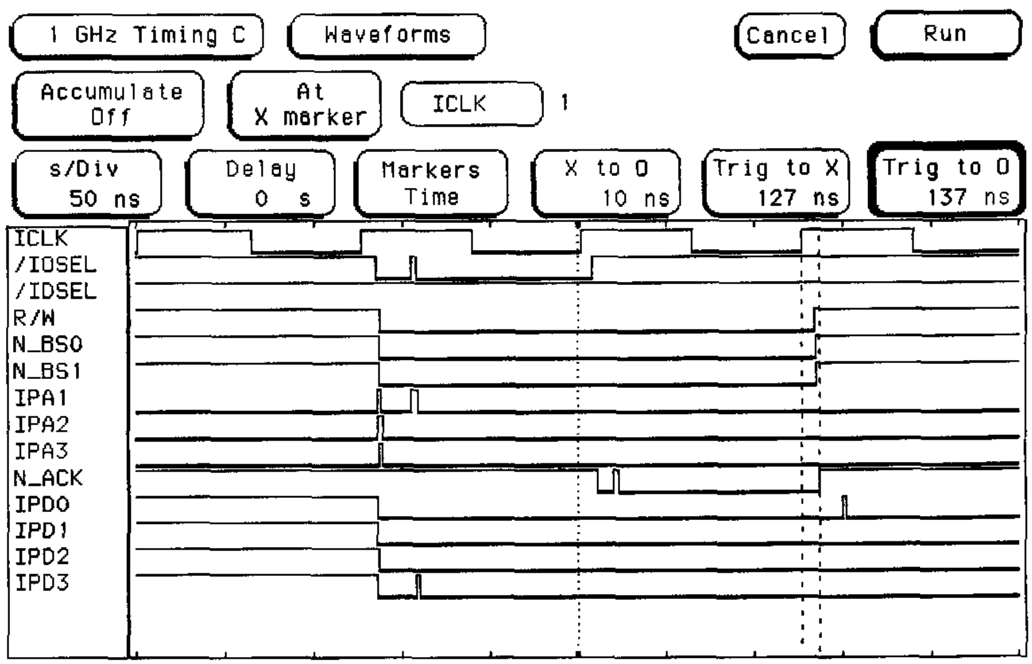

Figure 4-2 I/O Write at IPA = 0x00

Table 4-2 Wrong Power Supplies

Code)	Voltage Output (mV)	ΔV (mV)	Code)	Voltage Output (mV)	ΔV (mV)
0x800	00.2	6.9	0x812	43.0	0.3
0x801	07.1	4.6	0x813	43.4	0.4
0x802	11.7	6.1	0x814	43.6	0.2
0x803	17.8	2.2	0x815	44.4	0.8
0x804	20.0	10.0	0x816	44.6	0.2
0x805	30.0	3.1	0x817	44.9	0.3
0x806	33.1	3.4	0x818	45.2	0.3
0x807	36.5	0.9	0x819	46.7	1.5
0x808	37.4	1.8	0x81A	47.3	0.6
0x809	39.2	0.5	0x81B	48.4	1.1
0x80A	39.7	0.8	0x81C	49.1	0.7
0x80B	40.5	0.2	0x81D	51.0	0.9
0x80C	40.7	0.8	0x81E	51.7	0.7
0x80D	41.5	0.3	0x81F	52.6	0.9
0x80E	41.8	0.2	0x820	158.5	105.9
0x80F	42.0	0.1	0x821	166.5	8.0
0x810	42.1	0.1	0x822	171.8	5.3
0x811	42.7	0.6	0x823	179.0	7.2

NOTE: 4.8828 mV/bit is the theoretical ΔV

Similar mid-scale anomalies were noticed for 0 → +10, 0 → -10, -5 → +10, and +5 → -10 V ranges. However, quarter scale and full-scale codes yielded the expected outputs.

For the ±10 V range example, codes of 0x000, 0x400, 0x800, 0xC00, and 0xFFF yielded the expected results: -10.0 V, -5.00 V, 0.00 V, +5.00 V, and +10.0 V output, respectively.

☞ **NOTE**: Use external ±15 V supplies for any 10 V range usage.

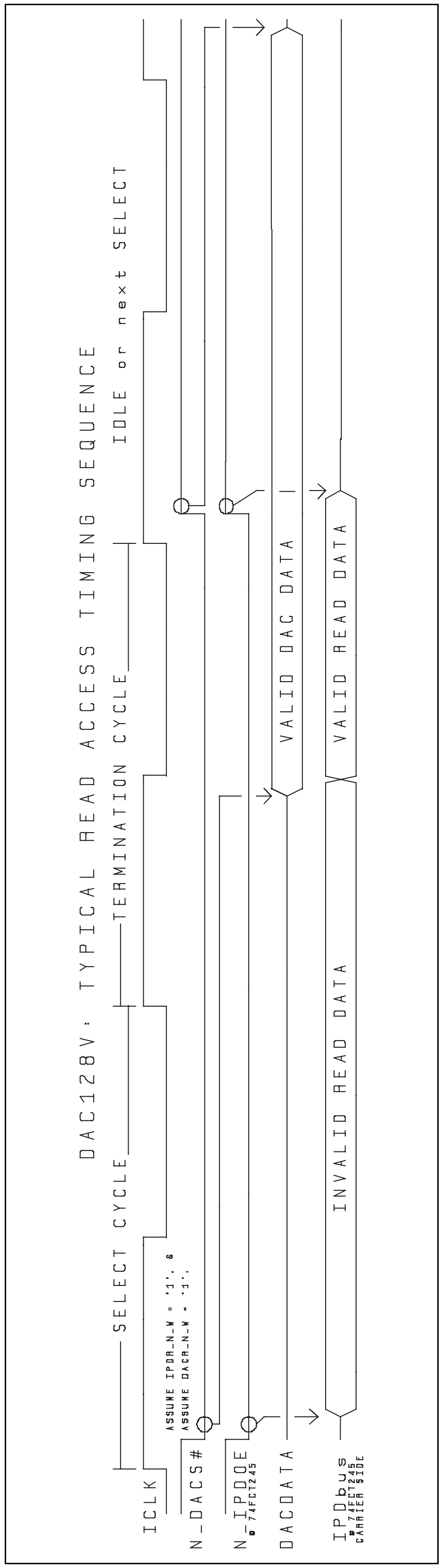

Figure 4-3 Typical Read Access Timing Sequence

4.5 Maximum Loads

The specification sheet for the DACs used on the DAC128V cites that the maximum current output for all analog channels is ±5 mA. However, a curve near the end of the data sheet presents information that indicates that the maximum capacity should be slightly over ±20 mA per channel. Two separate experiments were conducted to clarify the apparent discharging. To be safe, use ±5 mA as the typical peak loads, with confidence in knowing that you can get almost ±20 mA out if required.

The system configuration used to develop Table 4-3 is the same as that depicted in Figure 4-1. A 200.7 Ω resistor was placed, as a load to DAC01, across pins 2 and 3. DAC02 was left unloaded and was monitored at pin 6 of the I/O termination block. The DACs were run from ±15 V external supplies with their ranges set to ±10 V full scale.

Table 4-3 Fixed Overloads

Code	DAC02 Vout	DAC01 Vout	DAC01 Iout	Comments
0x000	-10.00 V	-4.15 V	20.7 mA	Flatlined overcurrent condition
0x200	-7.50 V	-4.15 V	20.7 mA	
0x400	-5.00 V	-4.15 V	20.7 mA	
0x480	-4.37 V	-4.14 V	20.6 mA	
0x4C0	-4.06 V	-4.05 V	20.2 mA	
0x500	-3.74 V	-3.73 V	18.6 mA	
0x600	-2.50 V	-2.494 V	12.4 mA	
0x700	-1.25 V	-1.247 V	6.2 mA	
0xFFF	+9.99 V	+4.26 V	21.2 mA	Flatlined overcurrent condition
0xF00	+8.75 V	+4.25 V	21.2 mA	
0xE00	+7.50 V	+4.25 V	21.2 mA	
0xD00	+6.25 V	+4.25 V	21.2 mA	
0xC00	+5.00 V	+4.25 V	21.2 mA	
0xB40	+4.06 V	+4.05 V	20.2 mA	
0xB00	+3.75 V	+3.74 V	18.6 mA	
0xA00	+2.50 V	+2.493 V	12.4 mA	
0x900	+1.25 V	+1.246 V	6.2 mA	
0x880	+0.624 V	+0.623 V	3.1 mA	
0x800	-0.30 mV	0.00 V	—	

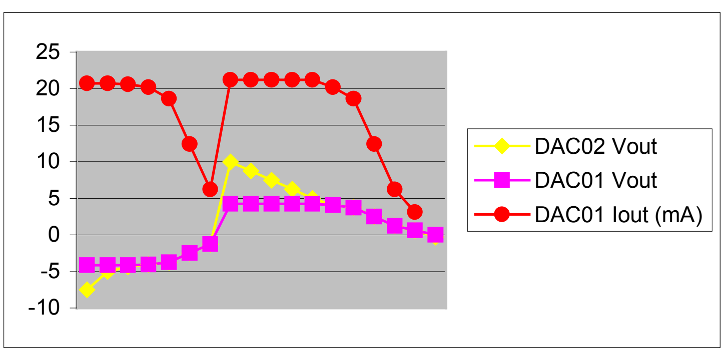

Figure 4-4 Flatlined Overcurrent Condition Chart

Table 4-3 clearly illustrates that there is a finite power limit for the DACs' buffered outputs and what happens to the voltage output when more current is requested than is deliverable. It does not give a clear picture as to what level of loading will deliver the proper voltage output for given code inputs at maximum, non-overcurrent loading conditions.

Table 4-4 was developed by decreasing the load resistance to that value, below which the voltage output begins to droop.

CAUTION: The mean for the last fourteen samples is 20.97857 mA with a standard deviation of 0.38946 mA. Note that this last test shows some droop near the positive rail. Therefore, use the DAC128V with loads exceeding ±5 mA with caution, after conducting capacity testing.

Table 4-4 Maximum Currents

Code)	DAC01 Vout	Load Resistance (Ω)	Load Current (mA)
0xFFF	+9.99 V	592.0	16.9
0xF00	+8.74 V	456.0	19.2
0xE00	+7.49 V	362.0	20.7
0xD00	+6.24 V	295.1	21.1
0xC00	+4.99 V	231.4	21.6
0xB00	+3.74 V	174.9	21.4
0xA00	+2.497 V	115.6	21.6
0x900	+1.247 V	58.3	21.4
0x800	0.00 V	N/A	N/A
0x700	-1.245 V	60.4	20.6
0x600	-2.494 V	121.6	20.5
0x500	-3.74 V	179.4	20.8
0x400	-4.98 V	237.1	21.0
0x300	-6.23 V	300.1	20.8
0x200	-7.48 V	356.0	21.0
0x100	-8.73 V	418.0	20.9
0x000	-10.00 V	493.0	20.3

4.6 Beyond Temperature

Table 4-5 presents a brief summary of a subset of data taken during product design verification temperature testing on four DAC128V boards loaded into a Motorola MVME162-01 and put into a temperature chamber.

Table 4-5 Extreme Temperature Performance

I/O Pin	Function	Voltage @ +25°C	Voltage @ -15°C	Voltage @ +85°C
For DAC128V #104 and DAC's Code = 0x000				
3	DAC01	-4.99	-4.99	-4.99
6	DAC02	-5.00	-4.99	-4.99
9	DAC03	-5.00	-4.99	-5.00
12	DAC04	-4.99	-5.00	-5.00
15	DAC05	-4.99	-4.99	-4.99
18	DAC06	-4.99	-4.99	-4.99
21	DAC07	-4.99	-4.99	-4.99
24	DAC08	-4.99	-4.99	-4.99
33	+10 Vout	+10.00	+10.00	+10.00
36	+5 Vout	+5.00	+5.00	+5.00
39	-5 Vout	-4.99	-4.99	-4.99
42	-10 Vout	-10.00	-10.00	-10.00
For Code = 0xFFF				
3	DAC01	+4.99	+4.99	+4.99
6	DAC02	+4.99	+4.99	+4.99
9	DAC03	+4.99	+4.99	+4.99
12	DAC04	+4.99	+4.99	+5.00
15	DAC05	+4.99	+4.99	+4.99
18	DAC06	+4.99	+4.99	+4.99
21	DAC07	+4.99	+4.99	+4.99
24	DAC08	+5.00	+5.00	+4.99

For each of five temperature points, 64 DAC voltage output readings and 16 reference voltage outputs were recorded with no load applied. The shortened table is presented to provide the user assurance that the DAC128V can handle wide temperature extremes while maintaining a high degree of accuracy.

Table 4-5 was developed using the carrier's 12 V supplies and the DACs were set up for 5 V full-scale range operations.

4.7 Slew Time Tests

While the specification sheet indicates that the DAC128V outputs typically settle within 6 µs, and ramp at a rate of 2.2 V/µs, the parameters are not always representative of those that may be encountered in practical applications.

Figure 4-4 presents one of 66 DSO diagrams that were captured for the generation of Table 4-6. The top trace (“D1”) is the N_ACK logic signal where the trigger was set up for the falling edge. The bottom trace presents the DAC’s voltage output

NOTE: The plateau that exists where the voltage is passing through 0 V was found to be typical for many large “step” changes, especially when heavily loaded.

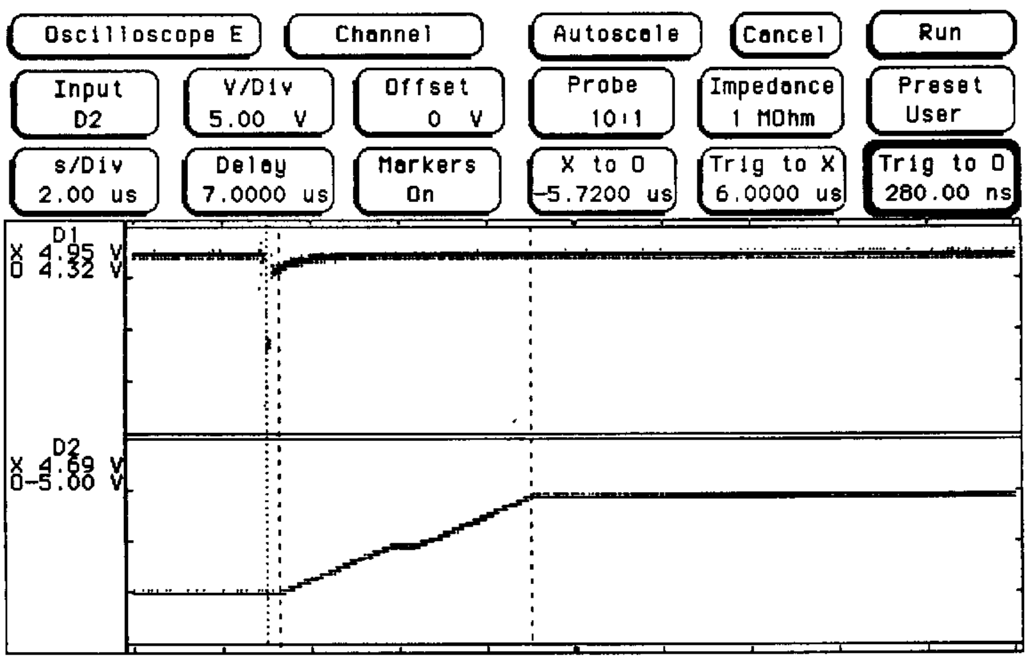

Figure 4-5 Typical Slew-Time Waveform

Table 4-6 Slew Time Tests

Load:			269 Ω*	677 Ω	5.54 KΩ	No Load
Change	**Code (hex)**	**Voltage**	**Time (µs)**			
Full Scale	000 → FFF	-9.99 → +9.99	—	11.48	9.96	9.08
	FFF → 000	+9.99 → -9.99	—	10.24	9.12	9.04
¾ Scale	000 → C00	-9.99 → +4.99	—	8.88	7.60	6.92
	C00 → 000	+4.99 → -9.99	—	8.16	7.00	7.08
	400 → FFF	-4.99 → +9.99	—	8.00	7.60	6.92
	FFF → 400	+9.99 → -4.99	—	7.32	6.92	6.92
½ Scale	000 → 800	-9.99 → 0.00	—	5.68	5.20	4.68
	800 → 000	0.00 → -9.99	—	5.24	4.72	4.96
	800 → FFF	0.00 → +9.99	—	5.00	4.72	4.72
	FFF → 800	+9.99 → 0.00	—	4.68	4.40	4.92
	400 → C00	-4.99 → +4.99	6.88	5.72	5.28	4.60
	C00 → 400	+4.99 → -4.99	6.00	5.20	4.76	4.88
¼ Scale	000 → 400	-9.99 → -4.99	—	3.16	2.40	2.36
	400 → 000	-4.99 → -9.99	—	2.72	2.08	2.84
	400 → 800	-4.99 → 0.00	3.36	3.84	3.24	2.56
	800 → 400	0.00 → -4.99	4.52	4.04	4.12	4.28
	800 → C00	0.00 → +4.99	2.64	2.36	2.40	2.24
	C00 → 800	+4.99 → 0.00	2.32	2.16	2.24	2.96
	C00 → FFF	+4.99 → +9.99	—	2.40	2.36	2.36
	FFF → C00	+9.99 → +4.99	—	2.04	2.24	2.80

* The 269 Ω load, the codes were limited for ±5 V outputs maximum to avoid overcurrent conditions; hence the fourteen non-applicable table positions with the "—" entries.

For a small change under no-load conditions, code 0x800 → 0x820, the corresponding voltage change of 0.00 V → 0.156 V occurred in about 500 ns.

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements	1.800 inches x 3.900 inches x 0.303 inches (above board), 4.572 cm x 9.906 cm x 0.770 cm
Weight	1.056 oz., 29.93 grams
Board thickness	0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate	8 MHz
Wait cycles	None on any transfer types
Hold cycles	Supported on all valid transfer types
Address decoding	Complete (no partial)
I/O transfers	
Writes	16-bit
Reads	16-bit
I/O locations	Eight, 16-bit
Ports	8
Maximum read/write rate	4 MTransfers/second, sustained
ID transfers	8-bit read (only) Zero-fill on upper byte 12 bytes, including CRC
Systran's manufacturer's	ID = 0x45, = E ASCII
DAC128V's model number	0x69, = i ASCII
Cyclic Redundancy Check value	0xE8
Maximum read rate	4 MTransfers/second, sustained
Memory transfers	Not supported
Interrupt Vector transfers	Not supported
Interrupt requests	None generated
DMA activity	Not supported
Acknowledgment on unsupported transfer attempts	None generated

Memory read and write
Interrupt read
ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

All data registers power up at mid-scale (I/O read of '0x0800')
No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

Power: +5 Vdc @ 24 mA (typical no load)
+12 Vdc @ 24 mA (typical no load)
-12 Vdc @ 22 mA (typical no load)

PERFORMANCE CHARACTERISTICS

Electrical Characteristics: Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:
- Minimum... -0.5 V
- Maximum for digital........................... +7.0 V
- Maximum for analog........................... ±15.45 V

RECOMMENDED OPERATING CONDITIONS:

Supply voltage:
- Maximum for analog........................... +4.75 V → +5.25 V
- ±5 V range analog............................... ±11.5 V → ±15.0 V
- ±10 V range analog............................. ±12.5 V → ±15.0 V

Logic Interface... ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): .... 0°C to +70°C
Temperature (no bias, storage): .... -40°C to +85°C
Humidity (Non-condensing): .... 5% to 95%
Vibration (Operating): .... 10 G's RMS (10→55 Hz)
Shock (Operating): .... 50 G's maximum
Altitude (Operating): .... 10,000 feet, maximum

MEAN TIME BETWEEN FAILURES (MTBF)

MTBF .... 2,683,123 hours per MIL-HDBK-217F

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

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FIGURES

B.1 Overview

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the DAC128V IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 A Short Glossary Of Analog Signal Applications

The following typical applications were developed by using one or more channels on the DAC128V IP Module. Most of the analog output voltage reference configuration operations can be performed (within limits) by proper connections and software manipulations.

☞ **NOTE:** If the DAC128V is to be used with the voltage range at +10 V and/or -10 V, the user must supply the $\pm$15 V power source to the I/O connector and make the appropriate jumper selections. This is necessary due to the onboard DAC's requiring the reference voltage be at least 2.5 V below the power source. For example the +10 V range is only 2 volts under the carrier's +12 V source and will cause possible errors in the DACs operation. Therefore an external power source of $\pm$15 V is required to ensure proper operation.

B.2.1 Avionics Signal Simulations

This application example provides the user with one of many possible configurations for using the DAC128V as an analog output reference. Flight Simulators and Automated-Test-Equipment (ATE) systems require the need for simulation of many analog signals generated from the line-replaceable-units (LRUs) contained in most avionics navigation suites. Most avionics signals are directly proportional to a unit of measure (i.e., nautical miles per hour, feet per second squared, inches of mercury, etc.) via an analog voltage representation.

One example would be a barometric altitude signal from an LRU that would be represented by a 12-bit DAC with 10 feet of altitude per bit resolution. This would be represented as 2 raised to the 12th power times 10, for a total of 40,960 feet of absolute altitude. If the DAC128V were configured for 0 to +10 V outputs, the altitudes between 0 and 40,960 feet would equate linearly to the range of 0 to +10 volts (in 0.000244 volt increments).

Another example would be a range or distance-to-go signal that would be represented by a 12-bit DAC with 1 nautical-mile-per-bit resolution. This would be represented as 2 raised to the 12th power, for a total of 4096 nautical miles of absolute distance. Again with the DAC128V configured for 0 to +10 V outputs the distance between 0 and 4096 nautical miles would equate linearly to 0 to +10 V (in 0.00244 V increments). Similarly with the DAC128V configured for 0 to +5 V, a velocity or true-air-speed signal could have a resolution of 0.1 miles-per-hour (mph) per bit (which equals 0.00122 V increments), yielding 0 to 409.6 mph true-air-speed.

B.2.2 Automatic-Test-Equipment Applications

The DAC128V can be used as one element of the “Self Test” portion of an ATE system that requires the use of analog-to-digital conversion. The DAC128V can exercise ADCs in the ATE systems for system integrity or confidence tests. Figure B-1shows the DAC128V connected to one of Systran’s ADCs (BHAS-ADC128F1) in a VME-based test system.

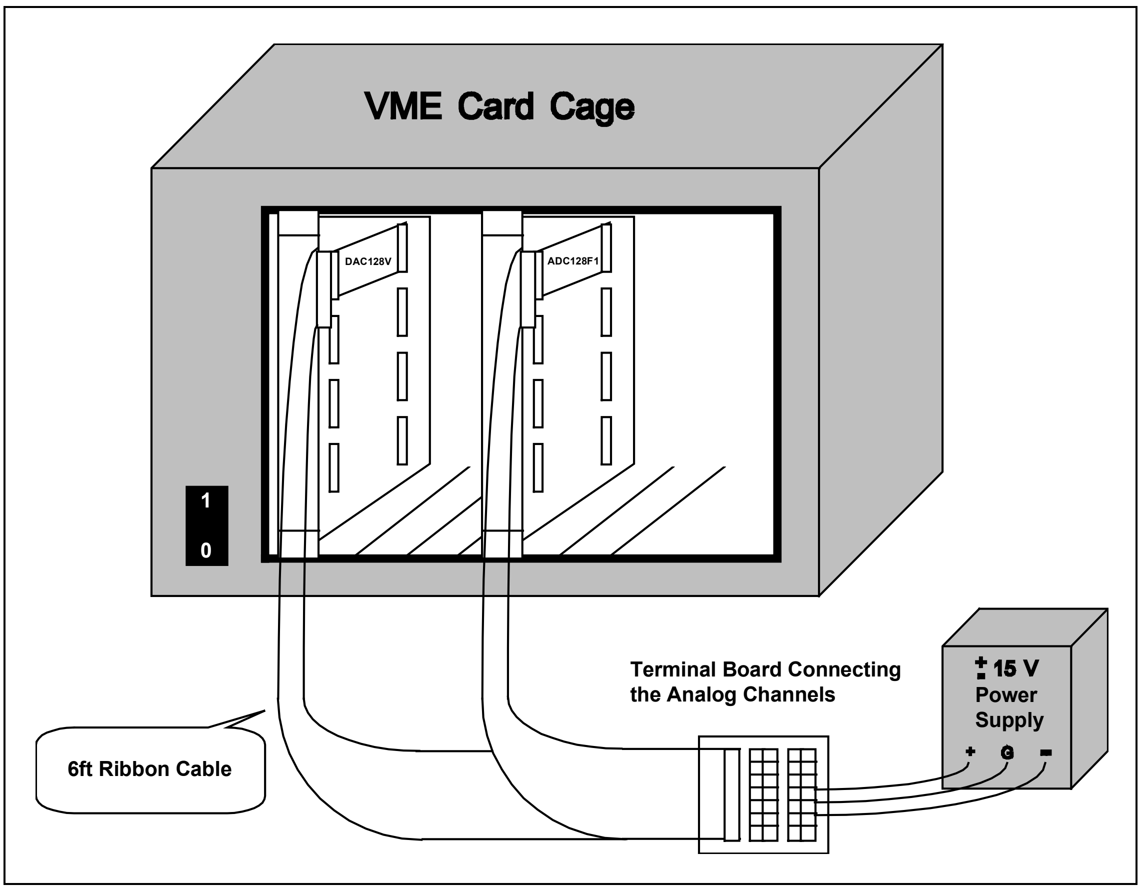

Figure B-1 DAC128V ATE Application

Figure B-2 shows the DAC128V connected to the ADC128F1 channel for channel, which then can be exercised across its +10 V, input voltage range. An external power supply is required for this application because the +10 V range, are used on the DAC128V.

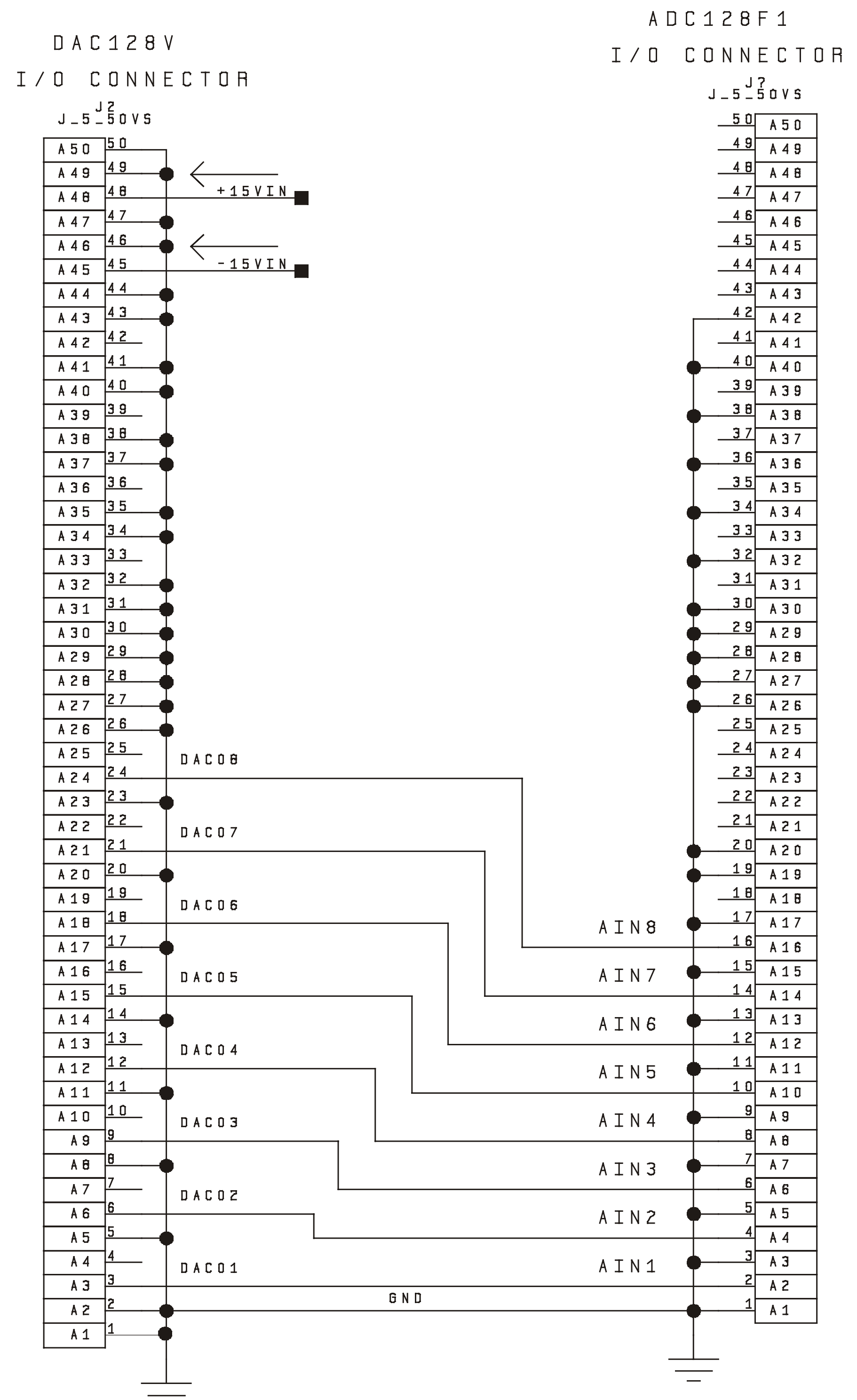

Figure B-2 DAC128V ATE Terminal Block Connection Schematic

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APPENDIX C

PROGRAMMING GUIDE

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TABLES

C.1 Overview

This section of the manual describes the operation of the DAC128V from the software perspective, detailing the DAC128V registers and providing programming examples. A more detailed description of the hardware can be found in Chapter 2, PRODUCT OVERVIEW, and in appendix B, TYPICAL APPLICATIONS.

C.2 Description

The DAC128V is a simple to use IP Module card with 8 channels of 12-bit digital to analog converters. The output ranges can be selected via a jumper for each group of four channels. Eight data registers, one per channel, set the output voltage for the channel. On power-up all data registers are set to '0x0800' (all channels at mid-range*)*.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information it presents. It saves space, lowers costs, improves reliability, and enables this IP Module to provide "no-wait" read accesses of this information.

☞ **NOTE**: The ID address space is fully decoded. Any attempt to access IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgment, and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane #0 (IPD[7:0]). The upper byte-lane #1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table C-1 is the DAC128V emulated ID Address Space PROM listing.

Table C-1 DAC128V ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII "I"	0x49
IPA = 0x01	ASCII "P"	0x50
IPA = 0x02	ASCII "A"	0x41
IPA = 0x03	ASCII "C"	0x43
IPA = 0x04	SYSTRAN's ID	0x45
IPA = 0x05	DAC128V's Model Number	0x69
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0xE8

C.4 IP Module I/O Address Map

The DAC128V's I/O Address Map is designed with efficiently located data registers in the IP Module I/O space (IPA = 0x00 ⇒ 0x07).

NOTE: The address detector circuitry is fully decoded. Any attempt to access IPA addresses at and above IPA = 0x08 will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The first location (IPA = 0x00) is the write-and-read-back Data Register 0 for the DAC output channel #1. Valid accesses to and from this location include: 16-bit writes, and 16-bit reads. All of the subsequent locations (IPA = 0x01 ⇒ 0x07) correspond to the DAC channels #1 through #8 respectively (where IPA = 0x01 is channel #2 - IPA = 0x07 for channel #8).

Table C-2 is the DAC128V I/O Address Map and contains the data register:

Table C-2 DAC128V I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	[XXXX] [11:8]	[7:0]	Data Register 0, Channel 1, 12-bits
IPA = 0x01	[XXXX] [11:8]	[7:0]	Data Register 1, Channel 2, 12-bits
IPA = 0x02	[XXXX] [11:8]	[7:0]	Data Register 2, Channel 3, 12-bits
IPA = 0x03	[XXXX] [11:8]	[7:0]	Data Register 3, Channel 4, 12-bits
IPA = 0x04	[XXXX] [11:8]	[7:0]	Data Register 4, Channel 5, 12-bits
IPA = 0x05	[XXXX] [11:8]	[7:0]	Data Register 5, Channel 6, 12-bits
IPA = 0x06	[XXXX] [11:8]	[7:0]	Data Register 6, Channel 7, 12-bits
IPA = 0x07	[XXXX] [11:8]	[7:0]	Data Register 7, Channel 8, 12-bits

C.5 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address
BASE + 0x0	BASE + 0x0	BASE + 0x2	IPA = 0x00
BASE + 0x2	BASE + 0x2	BASE + 0x6	IPA = 0x01
BASE + 0x4	BASE + 0x4	BASE + 0xA	IPA = 0x02
BASE + 0x6	BASE + 0x6	BASE + 0xE	IPA = 0x03
BASE + 0x8	BASE + 0x8	BASE + 0x12	IPA = 0x04
BASE + 0xA	BASE + 0xA	BASE + 0x16	IPA = 0x05
BASE + 0xC	BASE + 0xC	BASE + 0x1A	IPA = 0x06
BASE + 0xE	BASE + 0xE	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x1A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.6 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEbus Address	PC-AT Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x1	BASE + 0x0	BASE + 0x3	IPA = 0x00	0
BASE + 0x0	BASE + 0x1	BASE + 0x2	IPA = 0x00	1
BASE + 0x3	BASE + 0x2	BASE + 0x7	IPA = 0x01	0
BASE + 0x2	BASE + 0x3	BASE + 0x6	IPA = 0x01	1
BASE + 0x5	BASE + 0x4	BASE + 0xB	IPA = 0x02	0
BASE + 0x4	BASE + 0x5	BASE + 0xA	IPA = 0x02	1
BASE + 0x7	BASE + 0x6	BASE + 0xF	IPA = 0x03	0
BASE + 0x6	BASE + 0x7	BASE + 0xE	IPA = 0x03	1
BASE + 0x9	BASE + 0x8	BASE + 0x13	IPA = 0x04	0
BASE + 0x8	BASE + 0x9	BASE + 0x12	IPA = 0x04	1
BASE + 0xB	BASE + 0xA	BASE + 0x17	IPA = 0x05	0
BASE + 0xA	BASE + 0xB	BASE + 0x16	IPA = 0x05	1
BASE + 0xD	BASE + 0xC	BASE + 0x1B	IPA = 0x06	0
BASE + 0xC	BASE + 0xD	BASE + 0x1A	IPA = 0x06	1
BASE + 0xF	BASE + 0xE	BASE + 0x1F	IPA = 0x07	0
BASE + 0xE	BASE + 0xF	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 not applicable for ID Space

C.7 Data Registers 0-7 Bit Description (IPA = 0x00 ⇒ 0x07)

The DAC128V has eight 16-bit wide registers, each corresponding to a DAC channel. The DAC128V supports word (16-bit) reads and writes. The upper 4 bits are discarded during writes and are read back as zeros. The eight 16-bit read/write data registers are used to set the output voltage of the eight DAC channels. Data register 0 corresponds to DAC channel 1, register 1 to channel 2, ... register 7 to channel 8. On power-up all data registers are set to ‘0x0800’ (all channels at mid-range).

Table C-5 Data Registers Bit Descriptions

Bit #	15 to 12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	Not used	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
R/W	Read as 0's, Writes discarded.	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up state	N/A	1	0	0	0	0	0	0	0	0	0	0	0

D11 - D0: These bits comprise the 12-bit DAC value.

C.8 Programming Example

The following example illustrates how to program the DAC128V device. The power-up state is when all of the channels are set to their mid range. This example assumes that the output range is set to -5 V to +5 V. This example only interacts with channel 1; however, all of the channels work the same way.

- At power-up all the data registers values are ‘0x0800’ corresponding to 0.0 V.
- Write ‘0x0000’ to data register 0, DAC channel 1’s data register.
- The DAC channel 1 voltage output should now be -5.0 V.
- Write ‘0x0FFF’ to data register 0.
- The DAC channel 1 voltage output should now be +5.0 V.
- Write ‘0x0800’ to data register 0.
- The DAC channel 1 voltage output should now be 0.0 V.

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GLOSSARY

[x:y] --------------------------------- Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).

ATE ---------------------------------- automatic test equipment.

byte-lane ---------------------------- 8-bits of a data bus on octal boundaries.

CAE---------------------------------- Computer Aided Engineering.

DAC --------------------------------- Digital-to-Analog Converter.

doublewide ------------------------- An IP Module that is twice the size of the singlewide board.

EPLD -------------------------------- Erasable Programmable Logic Device.

ID PROM --------------------------- The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.

IP Module--------------------------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. An open industry standard defines the mechanical and electrical interface to the carrier board.

I/O ------------------------------------ Input/Output.

IP Module logic bus ------------- A synchronous, 8 MB/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6-bit wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

IPDbus------------------------------- IP Module Data Bus.

LRU---------------------------------- Line-replaceable units.

MTBF ------------------------------- Mean Time Between Failures.

ns, µs, ms -------------------------- Nanoseconds, Microseconds, and Milliseconds, respectively.

singlewide -------------------------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL ------------------------------- Very high speed integrated circuit Hardware Description Language.

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