SBS Technologies, Inc.

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# IP-Unidig

## IndustryPack Module With 24 Buffered TTL-Level I/O Lines

### Application Information

The IP-Unidig buffered digital I/O IndustryPack provides 24 flexible input/output signal lines with high current output drivers and wide voltage range inputs. Outputs will sink up to 64 mA of continuous load current. Inputs will handle up to +15/–5 V with a 1.25 V logic threshold for direct CMOS/TTL compatibility. Each line may be dynamically and individually configured for either input or output, providing maximum flexibility. Inputs and outputs may be double buffered, making the IndustryPack compatible with simulation systems requiring many inputs and outputs to be latched simultaneously.

Writing a one to any line turns off the output driver, allowing a passive pull up resistor to set the line to a logic high. Writing a zero to any line turns on the driver, driving the line to a logic low. For input use, a one is written to the corresponding line— this is the power up default. For output use, the binary value desired is written to the corresponding line.

Input and output lines may double buffered by providing an external clock. A bit in the Control Register selects the polarity of this clock, allowing inputs and outputs to be latched on either the rising or falling clock edge. The IP-Unidig-T is ideally suited for generating this clock, though any CMOS/TTL compatible clock source may be used.

The IndustryPack can function in a Master/Slave Mode for synchronizing multiple IndustryPacks. In this mode, the Master IndustryPack redrives the external clock source out I/O line 23. This line becomes the Master Clock, which should be wired to I/O line 24 on the Master and all Slave IndustryPacks.

Reset turns off the open collector output driver and sets disables double buffering for a consistent software interface.

A subroutine library and Windows NT drivers are available.

### Features

- 24 buffered TTL digital I/O lines on a single-wide IndustryPack
- 64 mA +15/-5 V operation
- Each line programmable as input or output
- Double-buffered input and output
- Cascadable external clock triggers double-buffering

## Specifications

| | |
|---|---|
| Form Factor | Single-wide Type I IndustryPack |
| IndustryPack Interface | Complies with ANSI/VITA-4 |
| Interface Speed | 8 MHz |
| Wait States | None |
| Number of Digital Lines | 24 individually programmable and input or output |
| Input Driver | +15/-5 V range<br>Logic threshold of 1.25 V with 50 mV hysteresis |
| Output Driver | Open collector transistor with 1 kOhm pullup<br>64 mA $I_c$ for $V_{ol}$=0.80 V |
| ESD Protection | None |
| Interrupts | None |
| Dimensions | 1.8 inches x 3.9 inches |
| Weight | 0.06 kg (0.1 lb) |
| Power Requirements (no load) | +5 VDC, 510 mA typ |
| Environmental | Operating temperature: -0 to +70°C<br>Humidity: 5 to 95% non-condensing<br>Storage: –40 to +85°C |

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## Ordering Information

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|---|---|
| IP-UNIDIG | IndustryPack with 24 buffered TTL-level I/O lines |
| EKIP50-UNIDIG | Engineering kit for IP-Unidig if mounted on a carrier with 50-pin ribbon cable header front panel I/O connectors. Contains:<br>Six foot 50 conductor ribbon cable (C-IP50F-IP50F-6)<br>Fifty screw terminal block with ribbon header (IP-TERM)<br>*(More items as below)* |
| EKHD50-UNIDIG | Engineering kit for IP-Unidig if mounted on a carrier with HD50 front panel I/O connectors. Contains:<br>Six foot cable HD50 male to HD50 male (C-HD50M-HD50M)<br>Fifty screw terminal block with HD50 female (IP-TERM-HD50)<br>*(More items as below)* |
| EKCM50-UNIDIG | Engineering kit for IP-Unidig if mounted on a carrier with Champ50 front panel I/O connectors. Contains:<br>Six foot Champ50 male to HD50 male cable (C-HD50M-CM50M)<br>Fifty screw terminal block with HD50 female (IP-TERM-HD50)<br>*(More items as below)* |
| All IP-UNIDIG engineering kits include: | Printed hardware user manual<br>Bill of materials<br>Board schematics<br>Assembly diagram<br>Motorola: MMPQ2369 data sheet<br>Motorola: 2N2369 data sheet<br>AMD: AM26LS33SC data sheet |
| QP-UNIDIG-DIG | QuickPack subroutine library for IP-Unidig. Contains:<br>Printed software user manual<br>Floppy Disk containing:<br>C source code<br>Release notes |
| ND-SDPACK | Windows NT 4.0 SDpacK IndustryPack driver CDROM |

## Associated Products

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| IP-UNIDIG-I | IndustryPack with 24 buffered TTL-level I/O lines and interrupts |
| IP-UNIDIG-I-ET | IndustryPack with 24 buffered TTL-level I/O lines and interrupts, extended temperature |
| C-IP50M-IP50M-3 | Three foot 50 conductor ribbon cable |
| C-IP50M-IP50M-6 | Six foot 50 conductor ribbon cable |
| C-CM50M-IP50M | Three foot Champ50 male to ribbon cable |
| C-HD50M-HD50M | Six foot HD50 male to HD50 male cable |
| C-HD50M-CM50M | Six foot Champ50 male to HD50 male cable |
| IP-TERM | 50 screw terminal block with ribbon cable connector |
| IP-TERM-HD50 | 50 screw terminal block with HD50 female connector |