

***16 CHANNEL, 32 BIT,  
40 MHZ "VME" UP/DOWN PRESETTABLE  
SCALER***

***MODEL VSC16***

***Joerger***  
ENTERPRISES, INC.

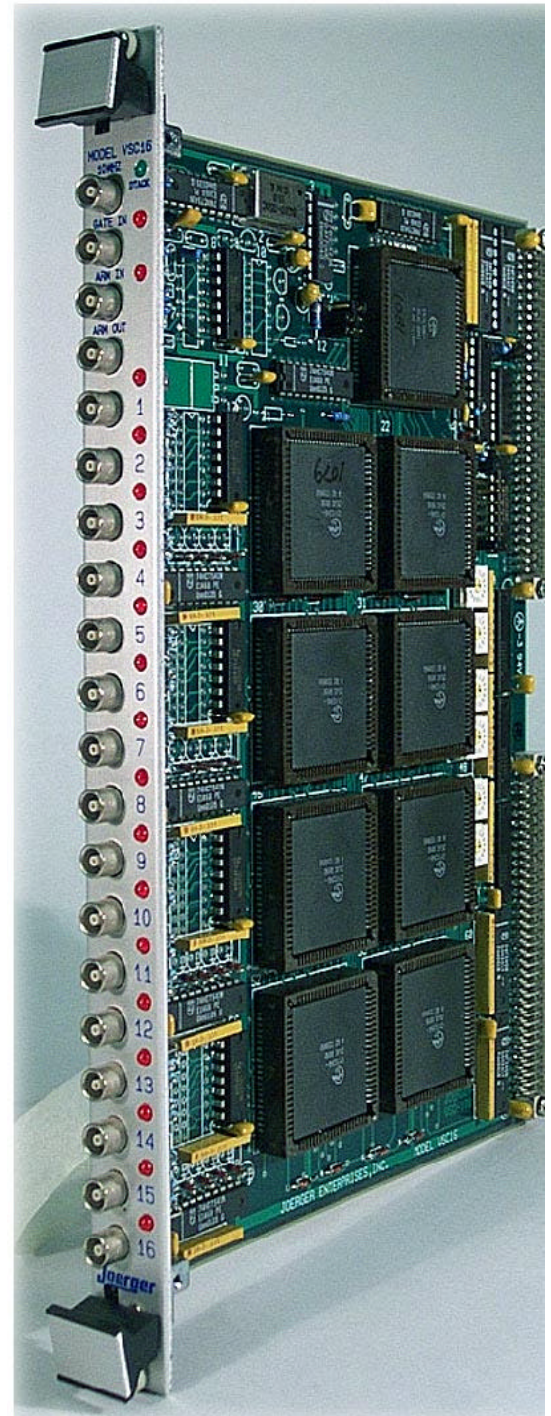
166 LAUREL ROAD, EAST NORTHPORT, NY 11731 U.S.A.

**16 CHANNEL, 32 BIT, 40MHZ "VME"  
UP/DOWN, PRESETTABLE SCALER**

**FEATURES:**

- 16 CHANNELS, 8 CHANNELS OPTIONAL
- 32 BIT CAPACITY
- 40 MHZ COUNTING SPEED
- TTL OR NIM COMPATIBLE
- UP/DOWN, PRESETTABLE COUNTERS
- COUNTING MODE INDIVIDUALLY SELECTABLE FOR EACH CHANNEL
- COMMON COUNTING GATE
- COMMON ARM CONTROL FOR IMPROVED SYSTEM PERFORMANCE
- INTERRUPT CAPABILITY WITH ACTIVE CHANNELS SELECTABLE
- SINGLE WIDTH, 6U, "VME" MODULE
- "EPICS" SOFTWARE COMPATIBLE

THE JOERGER ENTERPRISES, INC. MODEL VSC16 is a 16 channel, 32 bit, 40MHZ up, down, presettable scaler packaged in a single width "VME" module. Each channel is completely independent and its operating mode is preset in a rereadable register for verification. The module has an interrupt capability and each channel can be enabled or disabled from participating. The module has both a gate signal and arm signal to provide more complete system control. An arm output signal is provided that can be used to arm one or more units. The arm output signal is set when the module is



programmably armed and is reset by an internal stop signal, a counter reaching its preset condition, or a module reset. To visually indicate module operation LED's are provided for DTACK, GATE INPUT, ARM INPUT and an activity light for each channel to display if it is counting. A 10MHZ crystal oscillator output is also provided to perform such features as timing and testing. The module has onboard switches to set its address. The module is available for either TTL or NIM operation. To simplify system implementation "EPICS" software is available.

### ***SPECIFICATIONS:***

#### **SIGNAL INPUT, PER CHANNEL**

AMPLITUDE	Positive TTL standard Negative NIM optional
IMPEDANCE	50 OHMS, 500 OHMS optional
FREQUENCY	0 to 40MHZ, up/down programmable
CAPACITY	32 Bits, presettable

#### **GATE INPUT**

AMPLITUDE	Positive TTL input, 10K pull up standard, enabled Negative NIM optional
-----------	---

#### **ARM INPUT**

AMPLITUDE	Positive TTL input, 500 OHMS to ground, disabled. Negative NIM optional
-----------	---

#### **ARM OUTPUT**

AMPLITUDE	Positive TTL output standard, NIM output optional
-----------	---

#### **OSCILLATOR OUT**

	10 MHZ crystal osc. $\pm 0.01\%$ , TTL standard. NIM output optional.
--	---

### ***VME FUNCTIONS***

READ EACH CHANNEL

READ AND RESET EACH CHANNEL

PRESET EACH CHANNEL

READ/WRITE EACH CHANNEL FOR UP OR DOWN COUNTING

ENABLE OR DISABLE ARM OUTPUT

ENABLE OR DISABLE DISARM ON IRQ

ENABLE OR DISABLE EACH CHANNELS PARTICIPATION IN INTERRUPT GENERATION

IRQ RESET

READ MODULE IDENTITY, MANUFACTURER, MODEL, OPTIONS, AND SERIAL NUMBER

“VME” INTERFACE     A32/D32  
CONNECTORS         LEMO RA00250, MULTIPIN CONNECTOR OPTIONAL  
SIZE                 SINGLE WIDTH “VME” 6U CARD  
POWER                +5V, 2.4A: -12V, 330ma NIM OPTION  
OPTIONS:             1) 8 CHANNELS, VSC8  
                      2) NIM COMPATIBLE

JEI0102



166 LAUREL ROAD • EAST NORTHPORT, NY 11731, USA  
1-631-757-6200 • FAX: 1-631-757-6201 • Email: joerger@joergerinc.com • web:  
www.joergerinc.com

### **MODEL VSC, VME MULTICHANNEL SCALER**

The VSC8 contains eight 32 bit up/down scaler channels and the Model VSC16 contains 16 along with the VME bus interface. The board appears to the bus as a 256 byte block of addresses in extended memory only. Twelve addresses are used for status and control registers, accessible as bytes or words (except as noted). One hundred twenty eight addresses are used for data access for the scaler channels, accessible as LWORDS only. The AM codes for all access are 0Dh or 09h.

### **OPERATION**

#### **GENERAL:**

All the scaler channels are controlled by a common gate which is the "and" of the Gate input and the Arm input. On a TTL level VSC, both inputs must be high (for NIM level units both inputs must be low) for the scalers gates to be open (gate status is readable from control register). An Arm output, is provided to connect to the ARM input connector to allow one or many VSC's to be gated from the VME bus. The Arm out is set by accessing the control register and is reset by accessing the control register or by an overflow or under flow from an enabled channel (essentially an internal IRQ)\*. Each signal input (labeled 1-16 on front panel) has an LED associated with it that lights when it's channel is actively counting pulses. TTL scaler signal inputs are terminated with 50 ohms to ground and should be normally low (NIM version has 50 ohms to ground and inputs should be normally high). The TTL Arm input is terminated with 500 ohms to ground (NIM version has 50 ohms to ground) and if left open the Arm input is disabled. The TTL Gate input has a

10k ohm pullup to Vcc (NIM version has 10k to -5v and must be externally terminated if used) and if left open the Gate input is open (enabled).

Each channel can be individually reset, preset, set to count up or down or set to participate in interrupt generation. Interrupts can be generated while counting either up or down. (See descriptions and tables that follow).

## **INTERRUPT:**

The interrupt level is selected by two sets of on board jumpers. One jumper to select the bus IRQ line (IRQ1 to IRQ7 or none, IRQ1 is standard) and three jumpers to code the selected level into the IRQ Level/En Register (I1, I2, I4). These jumpers must match unless the IRQ line select jumper is in none. If the IRQ is enabled, (see control registers) and any unmasked channel overflows (counting up) or underflows (counting down), the IRQ is set. The interrupt is reset on acknowledge for an addressed IACK cycle (ROAK). It is also reset by a general reset or by writing to the IRQ reset address in the control/status register. The status of the IRQ can be checked by accessing the control register. The byte stored in the Status/ID Register (the Interrupt Vector) is returned with the acknowledge for the IACK cycle. Individual overflows are not latched, and no interrupt is latched if the module IRQ enable is not set.

## **FRONT PANEL SIGNALS:**

The module is available with TTL or NIM level signals. The description that follows is for a TTL unit. All input and output signals use single pin LEMO connectors. The 10MHZ connector is a TTL output which is from a +/-0.01% crystal oscillator. It is not gated and is for use as a timing signal or test signal. Gate and Arm In are TTL inputs used to gate all scaler channels. Both inputs must be high for the scaler gates to be open. An led for each of these inputs is provided. If both green led's are on, then the scaler gates are open. The Arm out TTL signal is provided to use as the Arm In to one or more VSC modules, it is controlled by 2 bits in the control register. Each signal input (labeled 1-16 on front panel) has an LED associated with it that lights when it's channel is actively counting pulses. TTL signal inputs should be normally low and the inputs are terminated with 50 ohms to ground.

## CONTROL AND STATUS REGISTERS (BYTE OR WORD ACCESS)

**RESET:** A complete reset of the module, the same as power up or SYSRESET, is done with a write to the base address. This will disarm, disable IRQ response, reset disarm on cout bit (allow enabled CH IRQ to disarm) reset mask register to zero (disable each channel's interrupt response) reset direction registers to zero (all channel count up) and reset all scaler channels to zero.

**CONTROL REGISTER:** Read or Write Arm status, and disarm on internal IRQ status.  
Read Gate status and IRQ status.

**DIRECTION REGISTER:** Read or Write direction for each channel using bit significant registers

**STATUS/ID REGISTER:** Read or write the Interrupt Vector (8 bits) for an IACK cycle

**IRQ LEVEL/EN REGISTER:** Read the IRQ level set with the on board jumpers I1, I2, and I4. Also one bit is used to enable or disable the board IRQ response.

**IRQ MASK REGISTER:** Read or write interrupt **IRQ MASK REGISTER:** Read or write interrupt participation enable or disable for each scaler channel using bit significant registers.

**IRQ RESET:** A Write cycle to this address resets the interrupt request F.F. without changing of Mask register or IRQ enable.

**SN REGISTER:** This register contains the VSC serial number (in hex) and is 1 byte, read only.

**MODULE TYPE REGISTER:** This register contains the module type identifier , 1 byte, read only.

**MANUFACTURER ID REGISTER:** This register is 1 byte, read only and contains 4A hex, ASCII "J".

**SCALER DATA:** Data is accessed as LWORD's (D32 only) from 2 blocks of 128 addresses. The first block is for read out of data only (base +80 to base +BF) and is read only. The second block of addresses (base +CO to base +FF) allows read and then reset for read cycles or preset for write cycles.

## VMEBUS ADDRESSING

The VSC occupies 256 bytes of extended address space (an A32 SLAVE). The board base address is selected using 6 hexadecimal switches and it can be selected on any 256 byte boundary in the extended address space (IC32 A08-A11 to IC51 A28-A31). Scaler data must be accessed using D32 cycles. Control/Status registers may be accessed using D8 (0) or D16 cycles. D16 access to 1 byte registers will return D8-D15 as a logic "0". BERR is not generated under any condition. The AM codes for all access are 0Dh or 09h.

### ADDRESS MAP

#### CONTROL/STATUS REGISTERS

##### ADDRESS

base +0h

RESET MODULE

WRITE ONLY

base +4h

CONTROL REGISTER

D0	0=DISARM (STOP)	1=ARM	R/W
D1	0=GATE CLOSED	1=GATE OPEN	Read only
D2	0=NO IRQ PENDING	1=IRQ PENDING	Read only
D3	0=DISARM ON INTERNAL IRQ	1=NO DISARM ON INTERNAL IRQ	R/W

NOTE: Internal IRQ is defined as and overflow (ct up) or underflow (ct down) from an enabled channel. The module enable IRQ bit can be enabled or disabled.

#### base +8h DIRECTION REGISTER (BIT SIGNIFICANT)

D0	CH1	0=UP	1=DOWN	R/W
D1	CH2	0=UP	1=DOWN	R/W
D2	CH3	0=UP	1=DOWN	R/W
D3	CH4	0=UP	1=DOWN	R/W
D4	CH5	0=UP	1=DOWN	R/W
D5	CH6	0=UP	1=DOWN	R/W
D6	CH7	0=UP	1=DOWN	R/W
D7	CH8	0=UP	1=DOWN	R/W
D8	CH9	0=UP	1=DOWN	R/W
D9	CH10	0=UP	1=DOWN	R/W
D10	CH11	0=UP	1=DOWN	R/W
D11	CH12	0=UP	1=DOWN	R/W
D12	CH13	0=UP	1=DOWN	R/W
D13	CH14	0=UP	1=DOWN	R/W
D14	CH15	0=UP	1=DOWN	R/W
D15	CH16	0=UP	1=DOWN	R/W

base +10h

STATUS ID/REGISTER

IACK cycle response byte W/R D0-D7



base +14h      IRQ LEVEL/EN REGISTER  
 IRQ LEVEL (coded)      READ ONLY      D0-D2

D0-D2	LEVEL
0	NOT USED
1	IRQ1 (As Shipped)
2	IRQ2
3	IRQ3
4	IRQ4
5	IRQ5
6	IRQ6
7	IRQ7

IRQ EN RESPONSE  
 D7      0=DISABLE IRQ      1=ENABLE IRQ      R/W

base +18h      IRQ MASK REGISTER (BIT SIGNIFICANT)

D0	0=DISABLE IRQ CH1	1=ENABLE IRQ CH1	R/W
D1	0=DISABLE IRQ CH2	1=ENABLE IRQ CH2	R/W
D2	0=DISABLE IRQ CH3	1=ENABLE IRQ CH3	R/W
D3	0=DISABLE IRQ CH4	1=ENABLE IRQ CH4	R/W
D4	0=DISABLE IRQ CH5	1=ENABLE IRQ CH5	R/W
D5	0=DISABLE IRQ CH6	1=ENABLE IRQ CH6	R/W
D6	0=DISABLE IRQ CH7	1=ENABLE IRQ CH7	R/W
D7	0=DISABLE IRQ CH8	1=ENABLE IRQ CH8	R/W
D8	0=DISABLE IRQ CH9	1=ENABLE IRQ CH9	R/W
D9	0=DISABLE IRQ CH10	1=ENABLE IRQ CH10	R/W
D10	0=DISABLE IRQ CH11	1=ENABLE IRQ CH11	R/W
D11	0=DISABLE IRQ CH12	1=ENABLE IRQ CH12	R/W
D12	0=DISABLE IRQ CH13	1=ENABLE IRQ CH13	R/W
D13	0=DISABLE IRQ CH14	1=ENABLE IRQ CH14	R/W
D14	0=DISABLE IRQ CH15	1=ENABLE IRQ CH15	R/W
D15	0=DISABLE IRQ CH16	1=ENABLE IRQ CH16	R/W

base +1Ch      IRQ RESET, clear and remove request      WRITE ONLY

base +20h      SERIAL NUMBER REGISTER      READ ONLY D0-D7 (in hex)

base +24h      MODULE TYPE (coded)      READ ONLY D0-D7

	VSC8	VSC16
TTL	8	16
NIM	9	17

Values are decimal

base +28h      MANUFACTURER ID      READ ONLY      D0-D7  
 returns 4Ah, ASCII "J"

**SCALER DATA ACCESS (D32 ONLY)**

CHANNEL	READ, WR=0	READ+RESET, WR=0 / PRESET, WR=1
CH1	base +80	base +C0
CH2	base +84	base +C4
CH3	base +88	base +C8
CH4	base +8C	base +CC
CH5	base +90	base +D0
CH6	base +94	base +D4
CH7	base +98	base +D8
CH8	base +9C	base +DC
CH9	base +A0	base +E0
CH10	base +A4	base +E4
CH11	base +A8	base +E8
CH12	base +AC	base +EC
CH13	base +B0	base +F0
CH14	base +B4	base +F4
CH15	base +B8	base +F8
CH16	base +BC	base +FC

Rev A: 02/25/02