BCG100

Bunch Clock Register Map

08	P0 Delay
06	Fine Delay
04	Ram Data
02	Ram Address
00	Control/Status Register

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write	P0 Delay															
Read	P0 Delay															
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write									Fine Delay							
Read									Fine Delay							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write	Ram Data															
Read	Ram Data															
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write									Ram Address							
Read									Ram Address							
	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Write														Disable Bunch Clock		
Read														Bunch Clock Disabld	P0 Detect	Running

Notes:

bunch-clock-reg.drw