APS Bunch Clock Generator

(Explanation of Storage Ring Bunch Clock Generator and System)

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1.0 Overview

The bunch clock generator (BCG) was designed and built by the ASD Controls Group for the APS Users (Fig. 1). It provides precise timing pulses for individual bunches of interest in the stored beam structure. These timing pulses are referenced to the storage ring (SR) revolution clock signals (P0) and the 351.8 MHz (352 MHz) rf signal from the low level rf (LLRF) system. The BCG100 module outputs can be adjusted in order to allow the User to vary the timing to reflect the position of a particular bunch of interest relative to P0, as well as to the physical location of the Users' experiment around the SR. This P0 signal originates in the main control room (MCR) as part of the Control "Master Timing System." The origin of the 352 MHz signal is the LLRF system. It is also distributed through the MCR as a part of the Control "Master Timing System."

1.1 Hardware

This BCG100 module is a single width VME card and can be resident in any IOC. It should be physically located as close as is practical to the experimental instrumentation that will be using the clock signal. The BCG100 module provides two output types for the User to choose from. A pulse output of ~1.5 ns is available at two places on the module's front panel, as well as a raw output of ~2.8 ns. For the BCG to work, a P0 clock signal is required and is provided by the revolution clock module located in the Controls IOC on top of the SR. The BCG system also needs an input from the rf

Fig. 1

BCG100

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systems' 352 MHz reference signal. Finally, the BCG100 module needs to be located in an IOC running EPICS, which is the system in which the support software operates .

1.2 Software

To control the BCG, the IOC in which it is resident must be running EPICS. This is necessary to access the software that has been developed to control the BCG. This software provides the various screens (Fig. 2) through which you can control the coarse and fine delay settings as described below. You can also enable or disable the output of the BCG from this screen. A status window is also provided on this screen, which tells you if the BCG is running or not as well as whether or not the P0 is detected. Also through EPICS, you can access the various displays that have been developed to plot the bunch position and number (Fig. 3).

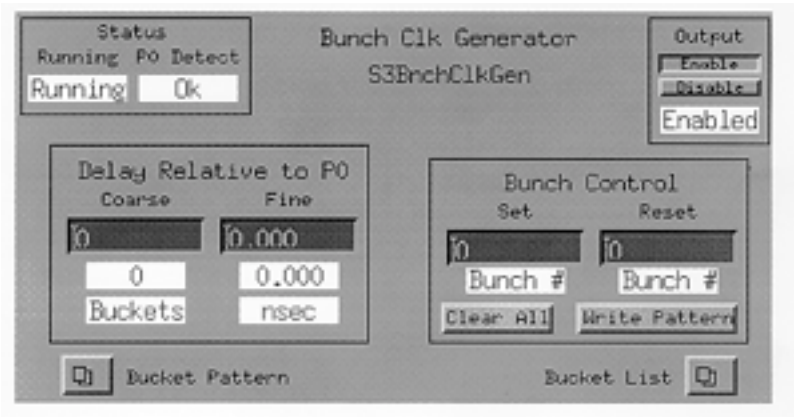

Fig. 2 - BCG100 EPICS Control Screen

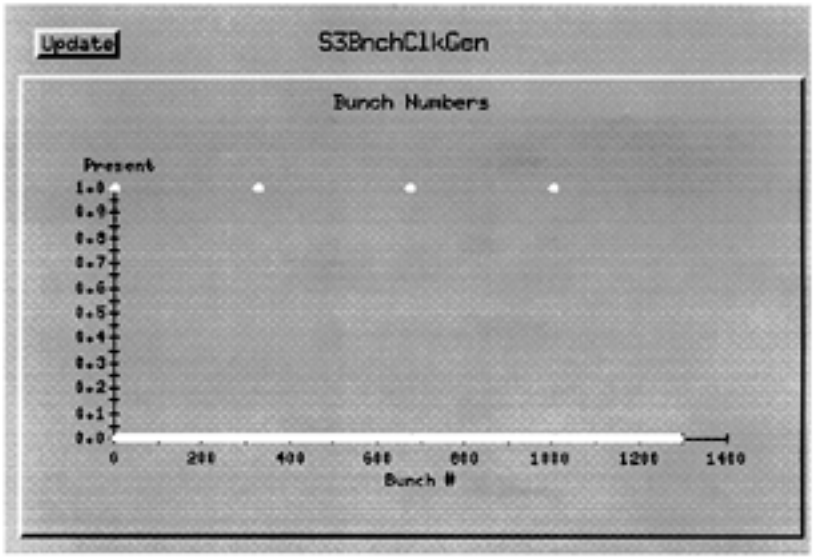

Fig. 3 - BCG100 Epics Display Screen

2.0 System Requirements

As mentioned above, the BCG100 is not a stand-alone module or system. It requires various inputs from other IOC-based modules, which deliver the timing and reference information needed for the BCG100 to operate. This information is input from the front panel and not over the IOC back plane. There are two modules required in addition to the BCG100 module. They provide the 352 MHz rf reference signal and a SR revolution clock signal (P0) that are required by the BCG100 module. Both of these modules have been designed and built by the ASD Controls Group for the APS. These are the TIM100 module and the FRX200 module. This system is shown in Fig. 4.

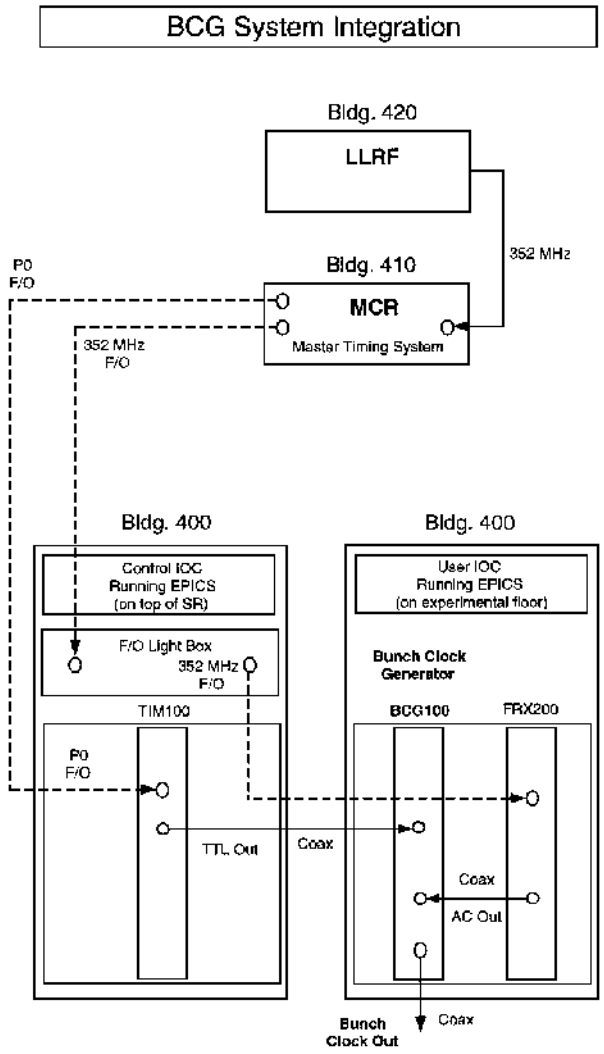

Fig. 4 - BCG100 System

3.0 Revolution Clock (P0)

The TIM100 module is a six-channel fiber-optic (F/O) input and TTL output converter module. Each channel has one multi-mode F/O input and provides one TTL output. Both the F/O input and the TTL output are accessible from the front panel (Fig. 5). The TTL output signal is not available on the VME back plane. The front end of this module, is modular and only those channels that are needed need be filled with front-end electronics. This option potentially minimizes the cost of the module.

4.0 Rf Timing Signal (352 MHz)

The other required module is the FRX200. It provides a 352 MHz F/O signal to electrical signal output. It has a single channel with an individual single-mode F/O input that then fans out to one ECL, one NIM and two AC coupled outputs (Fig. 6). All connections are on the front panel and are <u>not</u> available on the VME back plane. This module should be located in the same vicinity as the BCG100 for best performance.

5.0 MCR Inputs

The BCG requires two inputs provided from the MCR to produce its clock output (Fig. 4). The first of these signals is the P0 signal, and it is provided by ASD Controls Group. It originates in the MCR and is transmitted to the controls IOC crate located in each odd-number sector on top of the storage ring. It is brought out using multi-mode fiber-optic cable. This P0 signal fiber is run to the TIM100 module to provide a precise revolution counter clock signal. This is then routed to the BCG100 module using coax. The second required signal is the 352 MHz rf reference signal. Although the 352 MHz signal originates in the LLRF system, it is used and then distributed by the Controls Group as part of their "Master Timing System." This signal is brought out to the top of the storage ring to the Controls VME crate where the BCG100 is resident. This is done using high precision single-mode fiber to maintain the integrity of the signal. This fiber runs directly from the MCR to the F/O light box next to the Control System IOC crate in all the odd-numbered sectors. From this light box, a single-mode fiber jumper is used to connect to the FRX200 module in a VME crate. This F/O signal is converted to an AC signal and is then brought over to the BCG100 module using coax. To maintain signal integrity, the FRX200 and BCG100 should be located as close as possible to each other and to the final user of this clock signal.

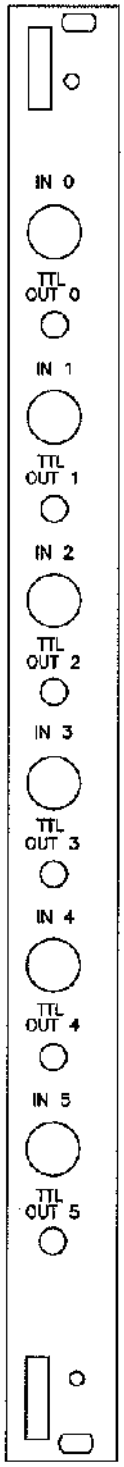

Fig. 5
Tim100

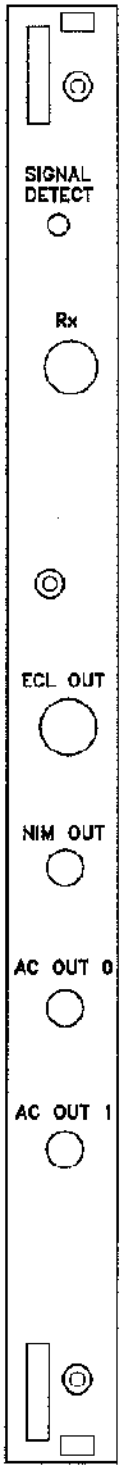

Fig. 6
FRX200

6.0 Control Environment (EPICS)

The software running in EPICS provides output delays relative to the P0, which is the precise clock signal that is generated by each revolution of the stored beam in the SR. Two ranges of delay are provided through the EPICS screens, which are shown above in Fig. 2. The first range is a coarse delay, which ranges from 0 to 1295 rf tics. An "rf tic" is equal to 2.8 ns. The second range is a fine delay, which ranges from 0 to 4.6 ns in 18.3 ps steps. There is also an area for "Bunch Control" in this window, but that is not accessible to Users. It is used only for Controls personnel to input bunch pattern information that is normally acquired over the IOC back plane. Other screens are provided by EPICS that plot the position of the bunches relative to the bunch of interest. An example is shown above in Fig. 3.

7.0 Performance

This performance information refers to the 352 MHz signal and is provided based on temperature-related changes, as well as on jitter. The following information is based on measured results except where stated otherwise:

- Temperature (@352 MHz, 23 degC ± 10 degC)
- Fiber Cable - 34 ps/degC/km (Helix LDF2-50 ~19 ps/degC/km calculated)
- Fiber Transmitter 7 ps/degC
- Fiber Receiver ~0 ps/degC
- BCG100 ~10 ps/degC (estimated worst case)
- Xmitr-Rcvr-525 m Cable - 16.5 ps/degC

The jitter information listed is within the limits of the test equipment available to measure it: less that 50 ps peak to peak.

8.0 Cost and Availability

At the time that this was prepared, there is only one BCG system in use, and there are no BCG100 modules on the shelf and ready for use. For this reason, those interested are encouraged to contact the APS/XFD User Office and request an estimate of how much time is required to obtain a module from the APS/ASD Controls Group. They will prepare for you a detailed proposal and cost estimate based on your requirements and location. A cost break down is provided as part of this estimate. If you have further questions, contact the APS/XFD User Office and we will provide you with the information or we will help direct you to the appropriate person(s) to provide you with a timely and concise answer.

9.0 BCG100 - External Connections

Connector	Type
• P0 In	SMB
• P0 Out	SMB
• 352 MHz In	SMA
• 352 MHz Out	SMB
• Raw Bunch Clk	SMB
• Bunch Clk A	SMA
• Bunch Clk B	SMB

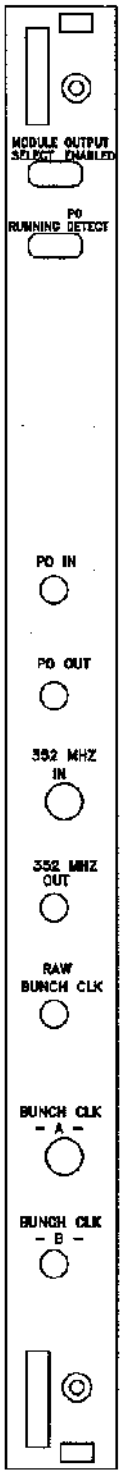

Fig. 7
BCG100