VMESC5

VME6U Slave 5-slot
IP Module Carrier
Hardware Reference Manual

Document No. B-T-MR-VMESC5##-A-0-A5

FOREWORD

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1. INTRODUCTION

1.1 Purpose

This document is a reference manual for Systran Corporation's VME6U Slave 5-Slot IP Module Carrier, part number BHAS-VMESC5. It provides a physical and functional description of the board and describes how to unpack, set up, install, and operate the hardware.

1.2 Scope

This manual covers the physical and operational description of the VMESC5, both from hardware and software perspectives. This manual also contains detailed technical information about the VMESC5's performance characteristics, and a few typical applications. You must have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules to effectively use this manual.

1.3 Style Conventions

1.3.1 Style Conventions

- Called functions are italicized: *OpenConnect()*
- Data types are italicized: *int*
- Function parameters are bolded: **Action**
- Path names are italicized: *utility/sw/cfg*
- File names are bolded: **config.c**
- Path file names are italicized and bolded: ***utility/sw/cfg/config.c***
- Hexadecimal values are written with the word hex italicized and following the value with a font size one smaller than the context: FB001040 *hex*
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded.

```
ls
file1          file2             file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/): /SYNC

1.4 Related Publications

- Systran I/O Products Technical Note #2001 entitled *Programmed Transfer Rate Analysis of the IP Module Bus Onboard the Motorola MVME162 Controller*
- *ANSI/VITA 4-1995* published by VMEbus International Trade Association, 7825 E. Gelding Drive, Suite 104, Scottsdale, AZ 85260-3415 USA.

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- E-mail: **support@systran.com**
- Fax: **(937) 252-1349**
- Word Wide Web address: **www.systran.com**

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2. PRODUCT OVERVIEW

2.1 Overview

This section describes the VMESC5 functions and features.

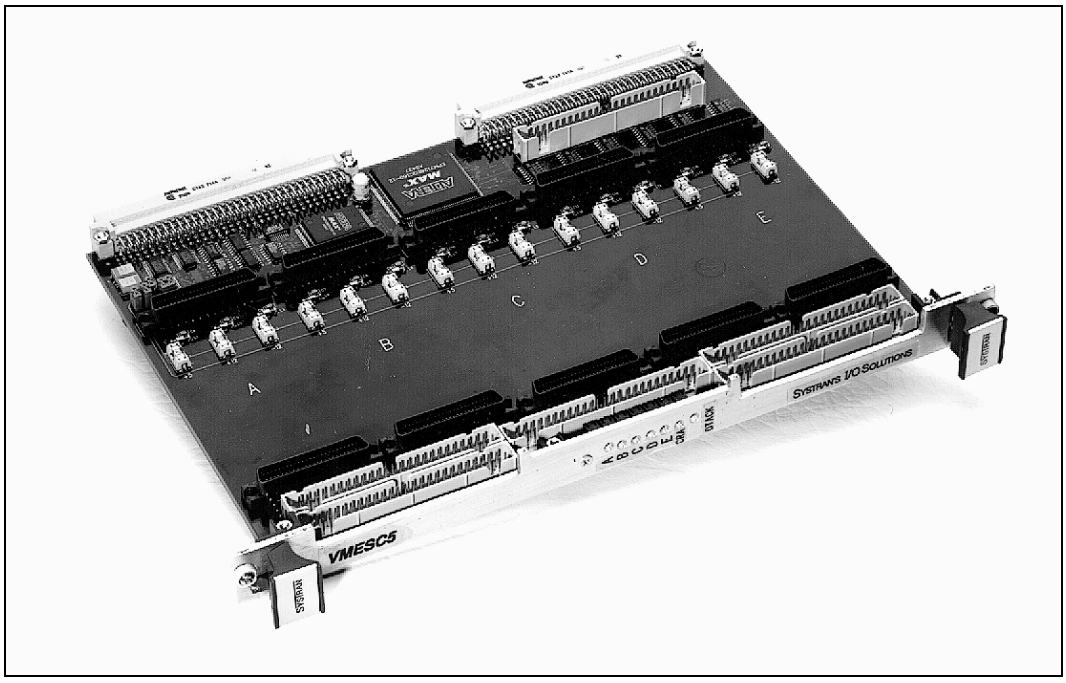

Figure 2-1 VMESC5 Board

2.2 Functional Description

The VMESC5 is a VME6U slave board that supports five singlewide IP Modules, three singlewide and one doublewide, or one singlewide and two doublewide IP Modules. This carrier is limited to the support of 8 MHz IP Modules. DMA and Memory accesses are not supported. All other IP Module transfer types, namely, ID, I/O, and Interrupt are supported. The following sections describe the board features, overall board layout, data transfer types, and detailed description of the registers. The VMESC5's VMEbus interface is designed in compliance with the *IEEE 1014-1987, VME Specification Revision C.1, Oct. 85*, and the IP Module's interface is designed in accordance with *ANSI/VITA 4-1995.*

NOTE: Physical doublewide IP Modules are supported. However, logical doublewide 32-bit transfers are not supported because memory transfers are not supported.

The VMESC5 was designed around a very easy to use, intuitive user interface, employing the highest quality (yet, reasonably affordable) components to provide the best performing, highest density VME6U IP Module slave carrier available. The VMESC5 is a super-synchronous design that does not insert IP Module hold cycles. This results in a very high throughput for this VME-to-IP Module bus coupling carrier.

The VMESC5 provides up to 250 I/O points (50 per IP Module) per VME6U slot with the entire area under the IP Modules as a solid ground plane to provide "quiet" operating conditions for sensitive analog IP Modules. The front panel LEDs give the user diagnostic information on accesses to the IP Modules, the VMESC5 local status and control registers, and the VME DTACK. The VMESC5 has a very easy to use and flexible VME interrupting capability where the individual interrupts from each IP Module can be programmed to assert any VME interrupt request signal.

NOTE: The extended implementation of write-transfer capability over the full ID addressing space for this product is over and above that described in the specification.

2.2.1 Features

- Up to 250 I/O points in a single, VME6U slot.
- Sustains 2.7 M transfers/second on READs and WRITEs (8- or 16-bit). *
- Each of 10 IP Module interrupt requests (2 per IP Module slot) can individually assert any of the 7 VME interrupt levels; equal levels IP Module slot prioritized.
- I/O, ID, and INT transfers with no HOLDs. *
- Read-Modify-Write cycles supported to IP Modules and VMESC5 registers.
- Independent field-replaceable fuses, and 'T'-type filters are used for the +5, +12, and -12 V power feeding each IP Module.
- IP Module error signals posted as status.
- IP Modules are individually software resettable.
- Board base address jumper selectable.
- Pure ground plane under IP Modules for "quiet" operation.
- Supports five singlewide, or three singlewide and one doublewide, or one singlewide and two doublewide IP Modules.
- Can connect IP Module Slot E I/O pins to VME P2 connector; doesn't lose IP Module slot usage for systems already using P2.
- Seven front-panel IP Module/Carrier Access and VME DTACK indicators (with pulse stretchers).
- Five 8-bit General Purpose registers.
- A16/D16/D8 VME transfers (2 KB block of space, address modifiers 29 *hex* and 2D *hex*).
- Supports writes to ID space.

* *ANSI/VITA 4-1995* used.

2.2.2 Accessories

IP Module Slot E I/O ribbon cable to the VME P2 connector (BHAS-RCVMEP2).

2.2.3 VME Memory Mapping Scheme

The mapping scheme of the ID and I/O address spaces for all five IP Modules, and the carrier's control and status registers are at fixed relative addresses from a jumper-selectable board base address. The board base address is selectable within the VME short I/O address space (A16) on 2 K boundaries. The VMESC5 responds to Address Modifier codes 29 *hex* and 2D *hex* corresponding to short non-privileged and short supervisory VME accesses, respectively. In Appendix B., Table B-1 shows the location of the ID and I/O spaces for each IP Module, and carrier-control register locations relative to the board base address.

2.2.4 ID Transfers

IP Module ID transfers are supported as A16/D16/D8 VME transfers. ID transfers are performed by a word or byte read/write operation of the slot IP Module ID address space from the VMEbus. The ID PROM values are located every other byte at odd-byte locations (IP Module byte lane 0). For word-reads the even byte is discarded. The ID PROM area allows read or write accesses to support future IP Modules requiring writes to the ID address space. Read-Modify-Write cycles are supported for ID transfers.

2.2.5 I/O Transfers

IP Module I/O transfers are supported as A16/D16/D8 VME transfers. I/O transfers are performed by a word or byte read or write operation of the slot IP Module I/O address space from the VMEbus. Even and odd single-byte reads are supported. Read-Modify-Write cycles are supported for I/O transfers.

2.2.6 Interrupt Transfers

Interrupts are requested by the IP Module by assertion of N_INTREQ0 or N_INTREQ1. An independent VME interrupter handles each of these IP Module interrupt request lines and asserts one of the seven prioritized VME interrupt request lines. This provides a minimum delay in asserting the interrupt request to the VMEbus master.

Which line is asserted depends on the interrupt level programmed into the carrier’s IP Module slot specific interrupt register. The five interrupt registers, one per IP Module slot, support independent selection of interrupt levels for both interrupt request signals N_INTREQ0 and N_INTREQ1. Upon receipt of the interrupt acknowledge from the VMEbus master, the VMESC5 will conduct a D8 transfer of the interrupt vector from the IP Module to the VMEbus. The interrupt request release will be dependent upon the individual IP Module being used.

2.2.7 Interrupt Prioritization

Interrupts in the VME system are prioritized in a two tier fashion; by Interrupt Request Level (IRQ) and relative position. This tier-effect is demonstrated in Figure 2-2.

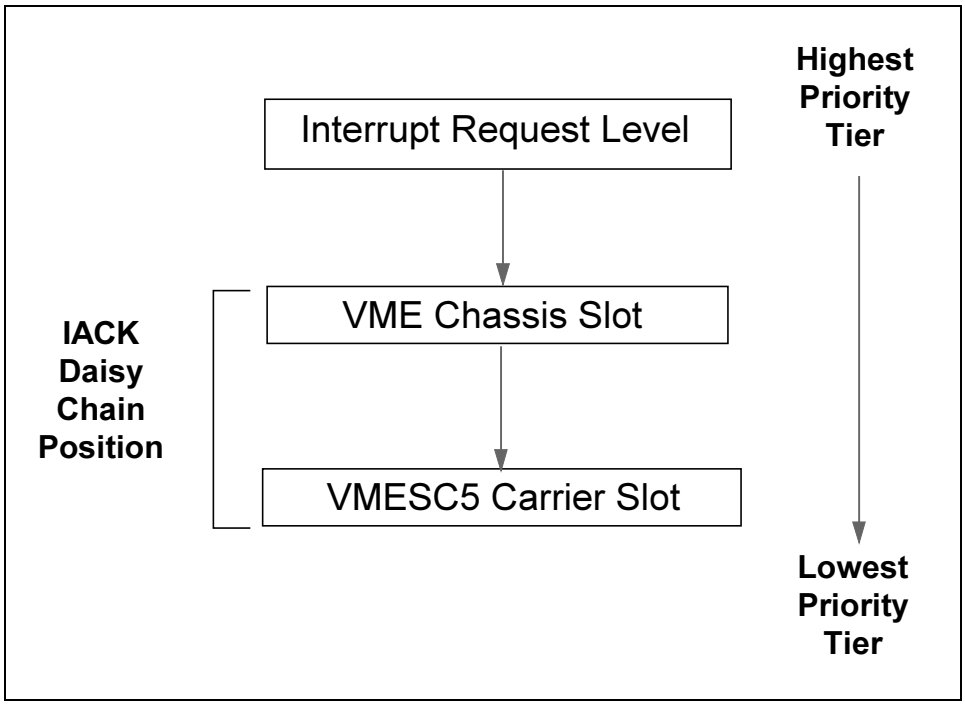

Figure 2-2 Interrupt Priority Tiers

The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest as shown in Table 2-1.

Table 2-1 Interrupt Request Level Priorities

INTERRUPT REQUEST LEVEL	PRIORITY
7	Highest
6	2nd Highest
5	•
4	•
3	•
2	2nd Lowest
1	Lowest

The second tier of prioritization is determined by the relative position in the interrupt daisy chain. The closer the interrupt requester is to the interrupt handler in the daisy chain, the higher its priority for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location (see Figure 2-3) and the IP Module slot location on the VMESC5 carrier (see Figure 2-4).

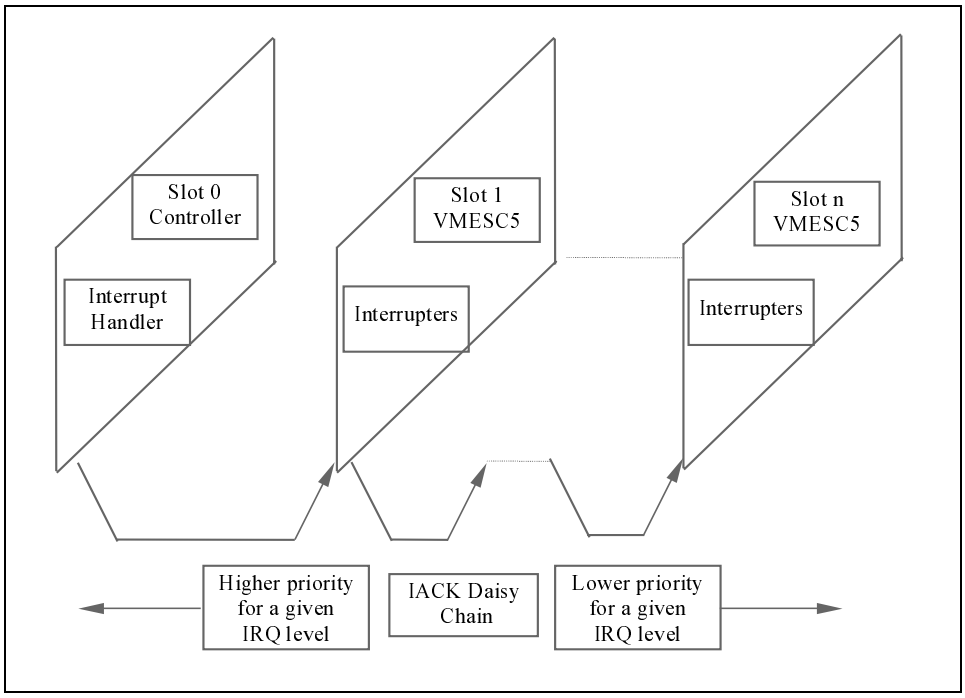

Figure 2-3 VME Chassis Slot Prioritization Through IACK Daisy Chain

The VMESC5 IP Module slot priority order from highest to lowest is A0, A1, B0, B1, C0, C1, D0, D1, E0, E1.

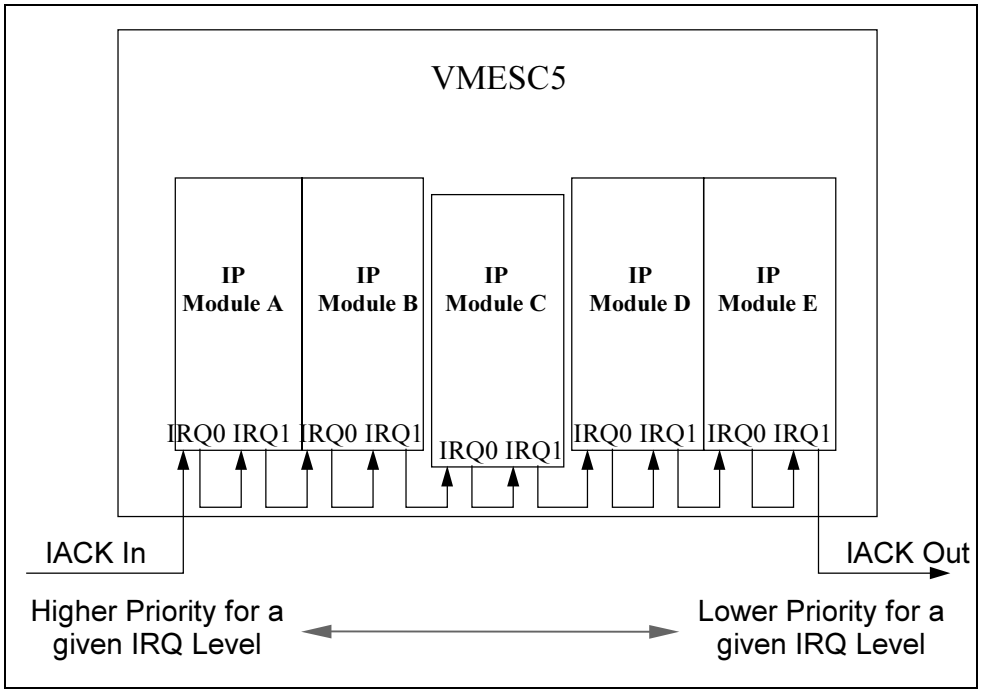

Figure 2-4 IACK Daisy Chain on the Carrier

2.2.8 General Purpose Registers

Five 8-bit general purpose user-defined registers are provided. Read-Modify-Write cycles are supported for general purpose register accesses.

2.2.9 Diagnostic LEDs

Seven diagnostic LEDS are located on the front panel of the VMESC5. Six of the LEDs, labeled A, B, C, D, E, and CRA, indicate when a read or write access is attempted to one of the five IP Module slots or the carrier registers. The seventh LED, labeled DTACK, indicates an acknowledgment by the IP Module or the VMESC5 of the attempted access. This scheme provides independent verification of the access and the acknowledgment.

2.2.10 IP Module Reset

Independent or simultaneous resetting of the IP Modules is facilitated through writes to the Reset register. Monitoring of the pulse-stretched reset signals is made possible by reading the Reset register. For a detailed description of this register see Appendix B.

2.2.11 Error Status

Monitoring of the IP Module ERROR signals is made possible by reading the Error Status register. For a detailed description of this register see Appendix B.

2.2.12 Strobe Signals

The IP Module STROBE signals can be connected via a 6-pin header (J17) located near the front panel.

2.2.13 Power Supply Filtering

Independent 'T' type filters are used for the +5, +12, and -12 volt power feeding each IP Module. Although this arrangement costs a little more, it provides superior power supply filtering.

2.2.14 Fuses

Independent field replaceable fuses are used for the +5, +12, and -12 volt power feeding each IP Module. Although this arrangement costs a little more, it provides superior short-circuit protection.

NOTE: Replacement fuses can be purchased directly from Littelfuse®, Inc. Phone (708) 829-0400.

1 Amp Fuse Manufacturer's Part Number R451001
2 Amp Fuse Manufacturer's Part Number R451002

2.3 Theory of Operation

Figure 2-5 is a simplified block diagram of the VMESC5 representing the signal flow between the VMEbus, IP Module Logic Bus and the IP Module I/O connectors. On the left side of the diagram is the VMEbus P1 connector through which all transfers between the VME host computer and the VMESC5's registers or IP Modules are conducted. The VMEbus transfers do not insert any IP Module hold cycles into the accesses to the IP Modules.

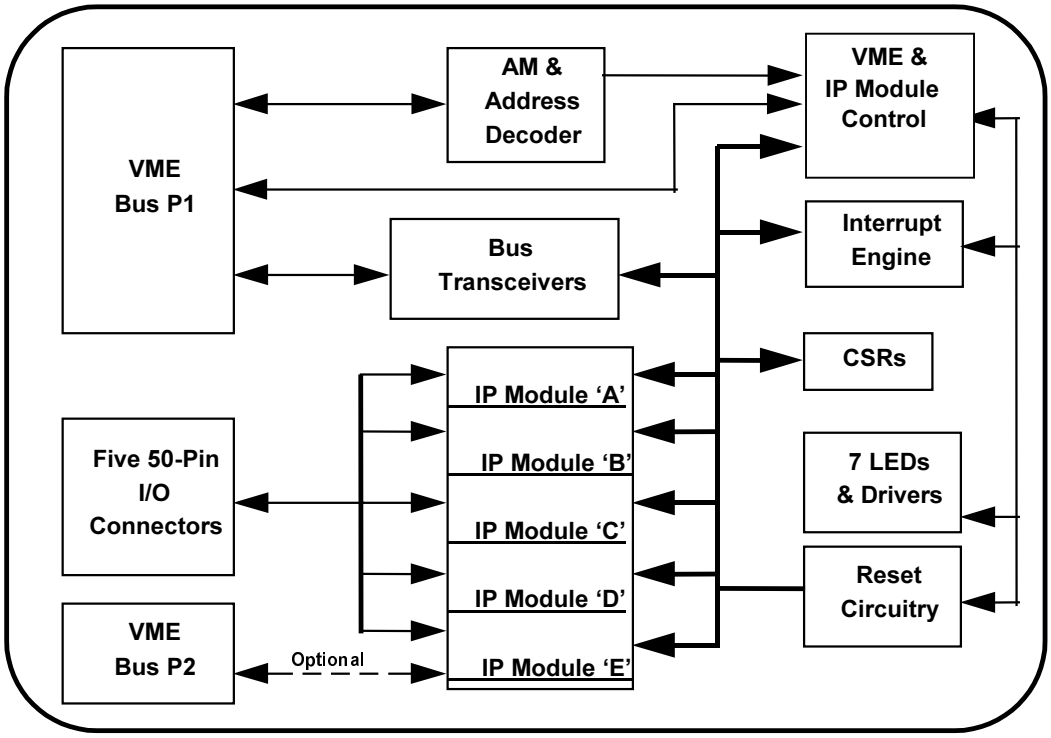

Figure 2-5 VMESC5 Block Diagram

The block labeled "AM & Address Decoder" handles decoding of the VME address and address modifiers. The block labeled "VME & IP Module Control" handles the transfer of data between the VME and both the VMESC5 CSRs and the IP Modules.

The block labeled "Interrupt Engine" controls the VME Interrupt requests, and prioritization of VME Interrupt Acknowledge cycles. The large block in the center of the diagram represents the five IP Module slots labeled IP Module 'A' down to IP Module 'E'. The IP Module I/O connectors are directly connected to the VMESC5's five front panel 50-pin I/O connectors. IP Module slot 'E' can be optionally connected to the VMEbus P2 connector via a short ribbon cable. The last two blocks at the lower right hand corner of the diagram contain the reset circuitry for each IP Module and drivers for each of the seven front panel LEDs.

The P1 connector is located on the upper left of the VMESC5 Assembly Drawing (Figure 2-6). When looking at the "top" or component side of the VMESC5, the IP Module slots are labeled from left to right for slot A through slot E. All of the I/O signals are connected through the five 50-pin connectors located at the bottom of Figure 2-6. (except the optional connection of slot E's I/O signals to the VME P2).

2.4 Functional Logic Module Overview

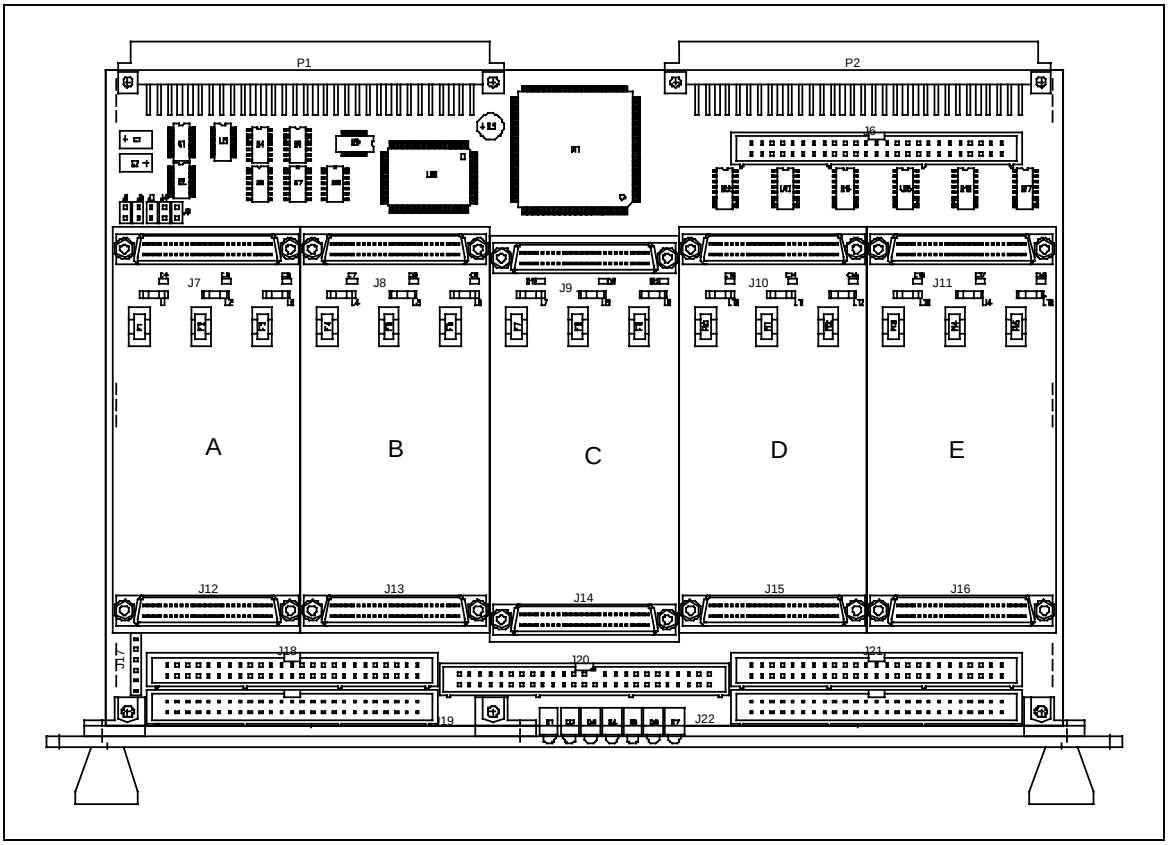

Figure 2-6 VMESC5 Mechanical Assembly

2.4.1 VMESC5 Module

The VMESC5 board has VHDL models that are sectioned into four functional logic blocks. Two of them are located in the VMESC5 module. The VMESC5 module works in conjunction with two other modules called VSC5INT and the V5LEDIPR module for driving the front panel LEDs and the IP Module's N_RESETx lines. All of the VHDL modules are defined below.

VME ADDRESS DECODER

This block detects VME host accesses to local VMESC5 Board Registers and IP Module I/O and ID spaces. An address-detect (HIT) signal corresponding to one of these address spaces is asserted when a matching address and address modifier (29 *hex* and 2D *hex*) is detected.

DATA TRANSFER ENGINE

The DTE handles the transfer of data between the VMEbus and the IP Modules. It monitors the HIT signals from the address decoders to determine when a transfer is to take place. The VME control signals and address lines provide the rest of the transfer information. The DTE asserts the appropriate IP Module ID or I/O select line and executes an IP Module synchronous transfer. The Reset and Error Status registers are also located in this module. The DTE is implemented using combinational logic and four state machines. The state machines include:

- One for VME Read cycles from the local control and status registers
- One for VME Write cycles to the local control and status registers
- One for IP Module I/O and ID Read cycles
- One for IP Module I/O and ID Write cycles

The IP Module read and write state machines complete a transfer in three IP Module clock cycles (six VME SYSCLOCK cycles). Specifically the IP Module READ state machine will place the data on the VMEbus upon detection of the appropriate IP Module acknowledge signal N_ACK, and the WRITE state machine will latch the data from the VMEbus and assert DTACK upon detection of the appropriate IP Module N_ACK signal.

REGISTERS

The VMESC5 module contains the Reset, Error Status, and General Purpose registers. For a detailed description of these registers, see Appendix B.

2.4.2 VSC5INT Module

VME INTERRUPT ENGINE

This module detects an interrupt request(s) from an IP Module(s), then asserts and selects VME interrupt request level(s). It monitors the VME V_IACKIN and A3-A1 signals and determines if the interrupt being acknowledged is the one it requested. If the level is different than the one requested, the acknowledge signal is passed on via V_IACKOUT daisy chain. If the acknowledge is for this IP Module's interrupt, the DTE asserts an internal interrupt HIT signal indicating that the corresponding IP Module's interrupt vector is to be transferred. If more than one IP Module interrupts at the same level and time, the interrupts are processed in a prioritized fashion. This scheme is from IP Module slot A's N_INTREQ0 as the highest priority, then slot A's N_INTREQ1 as the second highest, down to the slot E's N_INTREQ1 as the lowest. For a detailed description of interrupt prioritization, see section 2.2.7.

This interrupt priority scheme is implemented by the user programming a specific level in the interrupt level registers. The Interrupt Engine is implemented using combinational logic and three state machines. One state machine places an interrupt vector on the VMEbus just like a VME read cycle, one state machine for VME Read, and one for Write cycles to and from the local interrupt level registers. The IP Module Interrupt Acknowledge Cycle places the interrupt vector on the VMEbus in three IP Module clock cycles (six VME SYSCLOCK cycles). Specifically the IP Module interrupt vector state machine will place the vector on the VMEbus upon detection of the appropriate IP Module acknowledge signal N_ACK.

REGISTERS

The VSC5INT module contains the Interrupt Level registers for IP Module slots A through E. For a detailed description of these registers, see Appendix B.

2.4.3 V5LEDIPR Module

FRONT PANEL LED AND IP MODULE RESET DRIVERS

The V5LEDIPR module is responsible for monitoring all of the IP Module select signals from the VMESC5 module, combinationally driving the front panel LEDs from the one-shot drivers, and for logically “ORing” the VME system reset (V_SYSRESET) with the individual IP Module reset one-shot signals for driving each IP Module Reset signal.

3. INSTALLATION

3.1 Unpacking the VMESC5

Table 3-1 lists the contents of the VMESC5 shipping package.

Table 3-1 Contents of VMESC5 Shipping Packages

Qty	Description
1	VMESC5 Printed Circuit Assembly
1	Slot E I/O-to-VMEbus P2 Ribbon Cable (**Optional**) Systran Number: BHAS-RCVMEP2
2	Surface-mount spare fuses (one-1Amp, one-2Amp)
1	VMESC5 HW Reference Manual *

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number. (e.g. BTMR- VMESC5).

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

3.2 Visual Inspection of the VMESC5

Examine the VMESC5 to determine if any damage occurred during shipping.

3.3 VMESC5 Installation

NOTE: The VMESC5 is an Electrostatic Sensitive Device (ESD). Use an anti-static mat connected to a wristband when handling or installing the board.

The tools required for the VMESC5 installation are listed in Table 3-2.

Table 3-2 VMESC5 Installation Tools

QTY	DESCRIPTION
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

3.3.1 Installation of IP Modules on the VMESC5

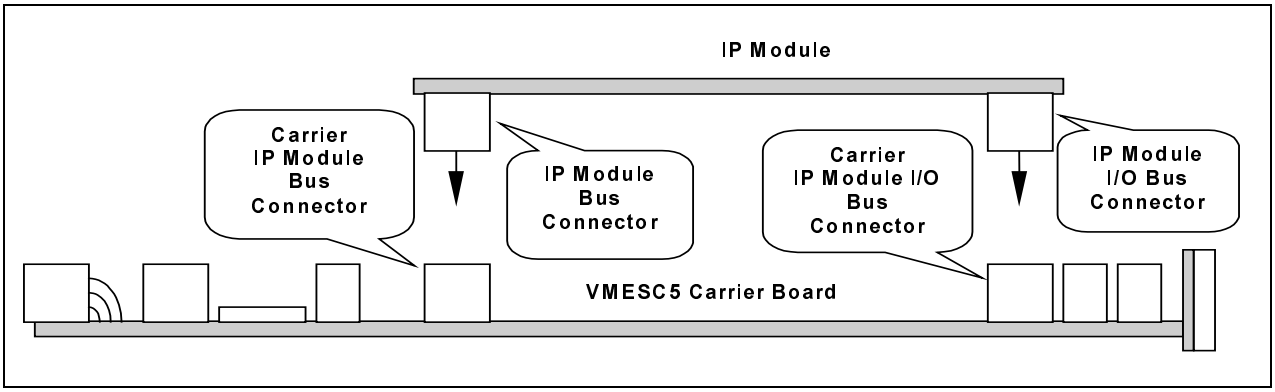

Figure 3-1 Installation of an IP Module on the VMESC5

Referring to the appropriate figures and table described below, perform the following steps in removing the VMESC5 from its shipping container (or from an existing installation) and installing IP Modules. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.

2a. Remove the VMESC5 from it's shipping container and move it to the ESD controlled area where the installation of the IP Module(s) can be made.

*2b. Remove the VMESC5 from the VME card cage and move it to the ESD controlled area where the installation of the IP Module(s) can be made.

3. Set the VMEbus base address on the J5-J1 jumpers (see Figure 3-2).

4. Install the IP Module(s) onto the carrier board by applying adequate and equal pressure to the IP Module(s) at both ends and the VMESC5 board (Figure 2-6).

*5. Install four M2x5mm flat head machine screws onto the IP Module's connectors.

*6. Install I/O cables necessary onto VMESC5.

*7. Install the Slot E I/O to VME P2 Ribbon Cable. **See warning below.

8. Install the VMESC5 into desired slot of a VME card cage.

WARNING: When the Slot E I/O-to-VMEbus P2 Ribbon Cable is installed, rows A and C of the VMEbus P2 are connected to the 50 I/O pins of slot E and cannot be used in systems with the P2 rows A and C used, but when the cable is NOT installed the VMEbus P2 connector is completely isolated from any on-board signals and can be used in VSB or VXI (with adapter) type systems.

3.3.2 VMESC5 VME Base Address

The VMESC5 VME board base address is set with five jumpers J5 - J1, corresponding to VME address bits A15 to A11, respectively. The board can be placed at one of 32 possible base addresses on 2 K boundaries.

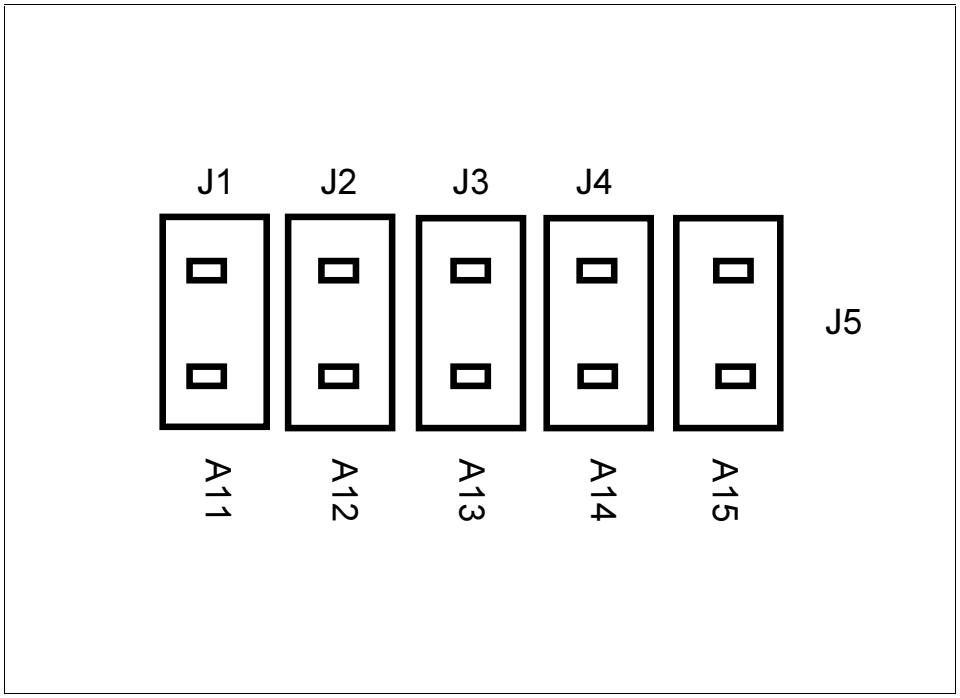

Figure 3-2 VMESC5 Jumpers J5 - J1

Placing a jumper across both posts corresponds to a logic low, or '0', for that address bit. Removing the jumper, or storing it on a single post, corresponds to a logic high, or '1', for that address bit.

NOTE: The VMESC5 is shipped with all jumpers installed and appears in memory at address 0000.

EXAMPLE:

The short I/O space on the MVME162 is located from FFFF0000 *hex* to FFFFFFFF *hex*, so the VMESC5 could be placed from FFFF0000 *hex* to FFFFF800 *hex* on 2 K boundaries.

Table 3-3 indicates all possible jumper settings for board base addressing.

For details of VME accesses to the VMESC5 on-board registers or IP Modules, see Appendix B.

NOTE: When using the MVME162 with OS-9, OS-9 maps the VMEChip2 GCSRs (Global Control Status Registers) to the beginning of short I/O space. This causes a bus conflict with boards placed at this address. To avoid a bus conflict:

1) do not put any VME boards at locations FFFF0000 *hex* to FFFF0010 *hex*;
2) move the GCSR location by changing the Group Select and Board Select values in the VMEChip2 LCSR registers (the 3 bytes starting at FFF4002C *hex*); or
3) disable the map decoder by writing an 'F *hex*' to the Board Select value (FFF4002E *hex*). Refer to the MVME162 manual for more details.

Also, OS-9 probes location FFFF10C0 *hex* for a disc controller on power-up. Locating a VME board at this address can cause unpredictable results..

Table 3-3 VMESC5 Board Base Address Jumper Selection Table

J5(A15)	J4(A14)	J3(A13)	J2(A12)	J1(A11)	VME Short I/O Address (hex)
ON	ON	ON	ON	ON	0000
ON	ON	ON	ON	OFF	0800
ON	ON	ON	OFF	ON	1000
ON	ON	ON	OFF	OFF	1800
ON	ON	OFF	ON	ON	2000
ON	ON	OFF	ON	OFF	2800
ON	ON	OFF	OFF	ON	3000
ON	ON	OFF	OFF	OFF	3800
ON	OFF	ON	ON	ON	4000
ON	OFF	ON	ON	OFF	4800
ON	OFF	ON	OFF	ON	5000
ON	OFF	ON	OFF	OFF	5800
ON	OFF	OFF	ON	ON	6000
ON	OFF	OFF	ON	OFF	6800
ON	OFF	OFF	OFF	ON	7000
ON	OFF	OFF	OFF	OFF	7800
OFF	ON	ON	ON	ON	8000
OFF	ON	ON	ON	OFF	8800
OFF	ON	ON	OFF	ON	9000
OFF	ON	ON	OFF	OFF	9800
OFF	ON	OFF	ON	ON	A000
OFF	ON	OFF	ON	OFF	A800
OFF	ON	OFF	OFF	ON	B000
OFF	OFF	OFF	OFF	OFF	B800
OFF	OFF	ON	ON	ON	C000
OFF	OFF	ON	ON	OFF	C800
OFF	OFF	ON	OFF	ON	D000
OFF	OFF	ON	OFF	OFF	D800
OFF	OFF	OFF	ON	ON	E000
OFF	OFF	OFF	ON	OFF	E800
OFF	OFF	OFF	OFF	ON	F000
OFF	OFF	OFF	OFF	OFF	F800

Where ON = logic ‘0’, OFF = logic ‘1’

3.3.3 Installation of I/O Cables

The VMESC5 provides easy access to all five IP Module I/O connectors. The I/O connectors are located near the front panel where standard 50-pin flat cables can be installed and routed out the edge of the front panel for easy system integration.

All of the VMESC5 IP Module I/O connector pin numbers directly correspond to each IP Module I/O pinout (i.e. a one-to-one relationship with pin 50 connected to pin 50 down to pin 1 connected to pin 1).

On the VMESC5:

- Connector J19 is the IP Module slot "A" I/O cable connector located at the upper left (facing front panel) of VMESC5 assembly drawing. It is the closest connector to the front panel at the top of the VMESC5 when installed (see Figure 2-6).
- Connector J18 is for IP Module slot "B" and is located just inside of J19.
- The I/O connector J20 is for IP Module slot "C" and is located in the middle of the VMESC5's front panel (see Figure 2-6).
- Connector J22 is for IP Module slot "D" and is the closest to the front panel at the lower left of VMESC5 assembly drawing. It is the closest connector to the front panel at the bottom of the VMESC5 when installed (see Figure 2-6).
- Connector J21 is for IP Module slot "E". It is the connector just inside of J22. This connector can be used normally like the other four I/O connectors being cabled out the front panel **OR** the IP Module slot "E" I/O can be brought out the VMEbus P2 connector via the IP Module slot "E" I/O accessory cable to J6 located next to the VMEbus P2.

Table 3-4 VMEbus P2 Row A & C Pin Assignments for the IP Module Slot E I/O

VMEbus P2 Pin #	Systran ROWa Signal	Systran ROWc Signal	VMEbus P2 Pin #	Systran ROWa Signal	Systran ROWc Signal
1	SLOTE_IO49	SLOTE_IO50	17	SLOTE_IO17	SLOTE_IO18
2	SLOTE_IO47	SLOTE_IO48	18	SLOTE_IO15	SLOTE_IO16
3	SLOTE_IO45	SLOTE_IO46	19	SLOTE_IO13	SLOTE_IO14
4	SLOTE_IO43	SLOTE_IO44	20	SLOTE_IO11	SLOTE_IO12
5	SLOTE_IO41	SLOTE_IO42	21	SLOTE_IO9	SLOTE_IO10
6	SLOTE_IO39	SLOTE_IO40	22	SLOTE_IO7	SLOTE_IO8
7	SLOTE_IO37	SLOTE_IO38	23	SLOTE_IO5	SLOTE_IO6
8	SLOTE_IO35	SLOTE_IO36	24	SLOTE_IO3	SLOTE_IO4
9	SLOTE_IO33	SLOTE_IO34	25	SLOTE_IO1	SLOTE_IO2
10	SLOTE_IO31	SLOTE_IO32	26	N/C	N/C
11	SLOTE_IO29	SLOTE_IO30	27	N/C	N/C
12	SLOTE_IO27	SLOTE_IO28	28	N/C	N/C
13	SLOTE_IO25	SLOTE_IO26	29	N/C	N/C
14	SLOTE_IO23	SLOTE_IO24	30	N/C	N/C
15	SLOTE_IO21	SLOTE_IO22	31	N/C	N/C
16	SLOTE_IO19	SLOTE_IO20	32	N/C	N/C

The short IP Module slot “E” I/O cable (Systran part number BHAS-RCVMEP2) is installed over the top of the IP Modules in slots “D” and “E”. Table 3-4 shows the pin assignments for the VMEbus P2 connector. The signals on the left side of the table, the P2 signals, and the signals on the right are those used by the IP Module slot E I/O connector.

NOTE: In Row B, the only pins used on the VMESC5 are pins 1,13, and 32 for +5 V and pins 2, 12, 22, and 31 for ground.

3.4 VMESC5 IP Module STROBE Connector

IP Module Logic Bus connector has a signal called “N_STROBE” and is user defined by the IP Module Logic Bus Specification. On the VMESC5 each of the strobe signals are provided through J17 with the IP Module slot “A” strobe signal on pin 1 through slot “E” on pin 5 with pin 6 grounded. Each of the strobe signals on the VMESC5 are pulled-up to +5 V via 10 KΩ resistors. The strobe connector (J17) is located at the upper left of the VMESC5 Assembly Drawing (which is at the top of the VMESC5 when installed).

Table 3-5 VMESC5 STROBE Connector Pin Assignments

Pin Number	Signal Name
1	N_STROBE_A
2	N_STROBE_B
3	N_STROBE_C
4	N_STROBE_D
5	N_STROBE_E
6	GROUND

Table 3-6 show the pin assignments for the VMEbus P1 connector. The signals on the left side are of the original VME specification signal nomenclature, and the signals on the right are those used by Systran.

Table 3-6 VMEbus P1 Rows A, B and C Pin Assignments

VMEbus P1 Pin #	VMEbus ROWa Signal	Systran ROWa Signal	VMEbus ROWb Signal	Systran ROWb Signal	VMEbus ROWc Signal	Systran ROWc Signal
1	D00	VMED0	BBSY*	N/C	D08	VMED8
2	D01	VMED1	BCLR*	N/C	D09	VMED9
3	D02	VMED2	ACFAIL*	N/C	D10	VMED10
4	D03	VMED3	BG0IN*	V_BG0IN	D11	VMED11
5	D04	VMED4	BG0OUT*	V_BG0OUT	D12	VMED12
6	D05	VMED5	BG1IN*	V_BG1IN	D13	VMED13
7	D06	VMED6	BG1OUT*	V_BG1OUT	D14	VMED14
8	D07	VMED7	BG2IN*	V_BG2IN	D15	VMED15
9	GND	GND	BG2OUT*	V_BG2OUT	GND	GND
10	SYSCLK	SYSCLK_IN	BG3IN*	V_BG3IN	SYSFAIL*	N/C
11	GND	GND	BG3OUT*	V_BG3OUT	BERR*	V_BERR
12	DS1*	VME_DS1	BR0*	N/C	SYSRESET*	V_SYSRESET_IN
13	DS0*	VME_DS0	BR1*	N/C	LWORD*	V_LWORD
14	WRITE*	VME_WRITE	BR2*	N/C	AM5	AM5
15	GND	GND	BR3*	N/C	A23	N/C
16	DTACK*	V_DTACK	AM0	AM0	A22	N/C
17	GND	GND	AM1	AM1	A21	N/C
18	AS*	V_AS	AM2	N/C	A20	N/C
19	GND	GND	AM3	AM3	A19	N/C
20	IACK*	V_IACK	GND	GND	A18	N/C
21	IACKIN*	V_IACKIN	SERCLK*	N/C	A17	N/C
22	IACKOUT*	V_IACKOUT	SERDAT*	N/C	A16	N/C
23	AM4	AM4	GND	GND	A15	VMEA15
24	A07	VME_A7	IRQ7*	V_IRQ7	A14	VMEA14
25	A06	VME_A6	IRQ6*	V_IRQ6	A13	VMEA13
26	A05	VME_A5	IRQ5*	V_IRQ5	A12	VMEA12
27	A04	VME_A4	IRQ4*	V_IRQ4	A11	VMEA11
28	A03	VME_A3	IRQ3*	V_IRQ3	A10	VMEA10
29	A02	VME_A2	IRQ2*	V_IRQ2	A09	VMEA9
30	A01	VMEA1_IN	IRQ1*	V_IRQ1	A08	VMEA8
31	-12V	-12V	+5VSTDBY	N/C	+12V	+12V
32	+5V	VDD	+5V	VDD	+5V	VDD

Table 3-7 shows the pin assignments for each IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran. The lower case "x" in the Systran signal name represents the "A", "B", "C", "D", or "E" mnemonic for each IP Module slot.

NOTE: The IP Module data bus, usually defined as IPD[15:0] for all of our IP Modules, is a subset of the information that appears on these signal lines. Since carrier register information also uses these signal lines, the bus was defined as the "VMESC5 Local Data Bus" designated as VLD[15:0].

Table 3-7 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names	Bussed or Unique	X = Pulled Up Via 10 KΩ Resistor
GND	50	GND	GND	GND
Reserved	49	RESERVED1	U	X
Ack*	48	N_IPxACK	U	X
A6	47	VMEA6	B	
Strobe*	46	N_STROBE_x	U	X
A5	45	VMEA5	B	
Intreq1*	44	N_IPxINTREQ1	U	X
A4	43	VMEA4	B	
Intreq0*	42	N_IPxINTREQ0	U	X
A3	41	VMEA3	B	
Error*	40	N_IPxERROR	U	X
A2	39	VMEA2	B	
DMAEnd*	38	N_DMAEND	U	X
A1	37	IPA1	B	
Reserved	36	RESERVED2	U	X
IOSel*	35	N_IPxIOSEL	U	
DMAck0*	34	N_DMACK0	U	X
IntSel*	33	N_IPxINTSEL	U	
DMAReq1	32	N_DMAREQ1	U	X
MemSel*	31	N_MEMSEL	U	X
DMAReq0	30	N_DMAREQ0	U	X
IDSel*	29	N_IPxIDSEL	U	
R/W*	28	V_WRITE	B	
+5V	27	+5VDC	+5 Vdc	+5 Vdc
GND	26	GND	GND	GND
GND	25	GND	GND	GND
+5V	24	+5VDC	+5 Vdc	+5 Vdc
+12V	23	+12VDC	+12 Vdc	+12 Vdc
-12V	22	-12VDC	-12 Vdc	-12 Vdc
BS1*	21	V_BS1	B	
BS0*	20	V_BS0	B	
D15	19	VLD15	B	X
D14	18	VLD14	B	X
D13	17	VLD13	B	X
D12	16	VLD12	B	X
D11	15	VLD11	B	X
D10	14	VLD10	B	X
D9	13	VLD9	B	X
D8	12	VLD8	B	X
D7	11	VLD7	B	X
D6	10	VLD6	B	X
D5	9	VLD5	B	X
D4	8	VLD4	B	X
D3	7	VLD3	B	X
D2	6	VLD2	B	X
D1	5	VLD1	B	X
D0	4	VLD0	B	X
Reset*	3	N_IPxRESET	U	
CLK	2	ICLK_x	B	
GND	1	GND	GND	GND

APPENDIX A
SPECIFICATIONS

Specifications

MECHANICAL

- Measurements:
  Length: 9.187 inches (23.33 cm)
  Width: 6.299 inches (15.99 cm)
- Weight: 9.984 oz., 283 grams (includes front panel)
- Board Thickness: 0.062 inches, 0.157 cm, nominally, (6 layers)

ELECTRICAL

- Power (No IP Modules installed): +5 Vdc (+5%) @ 0.53 Amps, +12 Vdc @ 0.0 Amps, - 12 Vdc @ 0.0 Amps

NOTE: The VMEbus ground and IP Modules' ground are not isolated through this board.

ABSOLUTE MAXIMUM SUPPLY RATINGS

- +5 Vdc Supply voltage with respect to ground: -0.5 Vdc minimum and +7.0 Vdc maximum
- +12 Vdc Supply voltage with respect to ground: Dependent on the IP Modules installed.
- -12 Vdc Supply voltage with respect to ground: Dependent on the IP Modules installed.

RECOMMENDED OPERATING SUPPLY RATINGS

- Supply Voltage with respect to ground: +4.75 Vdc to +5.25 Vdc

ENVIRONMENTAL SPECIFICATIONS:

- Temperature:
  (Operating): -0°C → +70°C
  (Storage): -65°C → +150°C
- Humidity (Noncondensing): 5% → 95%
- Vibration (Operating): 10 G's RMS, 20 Hz→2 kHz, random
- Shock (Operating): 50 G's maximum, all axes
- Altitude (Operating): 10,000 feet maximum

MEAN TIME BETWEEN FAILURE (MTBF):

- 667,245 hours per MIL-HDBK-217F

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APPENDIX B
PROGRAMMING GUIDE

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TABLES

B.1 Overview

This section describes the operation of the VMESC5 from the software perspective, detailing the VMESC5 registers, the overall mapping and addressing scheme for the board, and provides programming examples. A more detailed description of the hardware can be found in Chapter 2. and application concepts are discussed in Appendix D.

B.2 Description

The VMESC5 is an easy to use VME6U slave card that holds five singlewide, three singlewide and 1 doublewide, or 1 singlewide and 2 doublewide IP Modules. In addition to providing access to the I/O and ID space of the IP Modules via the VMEbus, the VMESC5 has 12 onboard control/status registers.

B.3 Board Base Address

The VMESC5 can be located anywhere in the VME short IO space (A16 space, address modifier codes 29 *hex* and 2D *hex*) on 2 K byte boundaries by setting the board base address jumpers. These jumpers, J1 to J5, correspond to address lines A11 to A15 respectively. For a detailed description of setting the board base address, see section 3.3.2.

B.4 Address Map

The IP Module IO and ID spaces, and the carrier's control and status registers, reside at a fixed relative address from the VMESC5 base address. Table B-1 shows the complete memory map for the board.

Table B-1 VMESC5 Address Map

Address Space or Register Name	VME Address (relative to board base address)	Size
IP Module A I/O	Base+000h	128 bytes
IP Module A ID	Base+080h	128 bytes
IP Module B I/O	Base+100h	128 bytes
IP Module B ID	Base+180h	128 bytes
IP Module C I/O	Base+200h	128 bytes
IP Module C ID	Base+280h	128 bytes
IP Module D I/O	Base+300h	128 bytes
IP Module D ID	Base+380h	128 bytes
IP Module E I/O	Base+400h	128 bytes
IP Module E ID	Base+480h	128 bytes
IP Module Reset Register	Base+500h - Word Access Base+501h - Byte Access	5 bits
Error Status Register	Base+502h - Word Access Base+503h - Byte Access	5 bits
IP Module A Interrupt Register	Base+580h - Word Access Base+581h - Byte Access	6 bits
IP Module B Interrupt Register	Base+582h - Word Access Base+583h - Byte Access	6 bits
IP Module C Interrupt Register	Base+584h - Word Access Base+585h - Byte Access	6 bits
IP Module D Interrupt Register	Base+586h - Word Access Base+587h - Byte Access	6 bits
IP Module E Interrupt Register	Base+588h - Word Access Base+589h - Byte Access	6 bits
General Purpose Register A	Base+600h - Word Access Base+601h - Byte Access	8 bits
General Purpose Register B	Base+602h - Word Access Base+603h - Byte Access	8 bits
General Purpose Register C	Base+604h - Word Access Base+605h - Byte Access	8 bits
General Purpose Register D	Base+606h - Word Access Base+607h - Byte Access	8 bits
General Purpose Register E	Base+608h - Word Access Base+609h - Byte Access	8 bits

B.5 Register Descriptions

The VMESC5 registers can be accessed as byte (D8) or word (D16) values. When accessed as words, the upper byte is not driven by the carrier and its value is all '1's due to VLD[15:8] pull-up resistors. The unused bits in the lower byte are driven as '0's on reads. All unused bits are discarded on writes. The hexadecimal VME addresses for the registers shown below are relative to the board base address and are in the format (WORD/BYTE) for word and byte accesses respectively.

B.5.1 Reset Register (500/501)

Setting one of the bits RES_E through RES_A to a one, asserts the corresponding IP Module's reset line. The bits can be set individually by writing a '1' to that bit or simultaneously with a single write of '1F' *hex*. When set, a one-shot is triggered supplying a minimum 200 ms reset pulse as required by the IP Module specification. When read, these bits return the status of the corresponding IP Module's reset line (a'0' means the IP Module is not being reset, a '1' means it is in a reset condition).

Table B-2 Reset Register Bit Description

Bit #	B15-B8	B7-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	RES_E	RES_D	RES_C	RES_B	RES_A
R/W	Reads '1's Writes discarded	Read '0's, Writes discarded	R/W	R/W	R/W	R/W	R/W
Power up State	N/A	N/A	0	0	0	0	0

NOTE: RES_E-RES_A: Reset bits for IP Module slots E to A.

B.5.2 Error Status Register (502/503)

These bits indicate the state of the corresponding IP Module N_xERROR. If the N_xERROR* signal is asserted (active low) for a particular IP Module, then the corresponding ERR_N bit will be set to a '1'. If the error signal is not asserted, then the corresponding bit will be cleared.

Table B-3 Error Status Register Bit Description

Bit #	B15-B8	B7-B5	B4	B3	B2	B1	B0
Bit Name	Not Used	Not Used	ERR_E	ERR_D	ERR_C	ERR_B	ERR_A
R/W	Reads '1's Writes discarded	Reads '0's Writes discarded	R	R	R	R	R
Power up State	N/A	N/A	State of IP Module E ERR* Signal	State of IP Module D ERR* Signal	State of IP Module C ERR* Signal	State of IP Module B ERR* Signal	State of IP Module A ERR* Signal

NOTE: ERR_E-ERR_A: Error Status bits for IP Module slots E to A.

B.5.3 Interrupt Level Registers A to E (580/581 to 588/589)

The three interrupt level bits, IL2-IL0, determine the interrupt request level that will be asserted on the VME bus when the corresponding IP Module IRQ line is asserted. Valid interrupt levels are 1 to 7. A value of '0', not a valid interrupt request level, will not assert a VME interrupt request. Thus, a value of '0' can be written to these registers to disable interrupts.

The interrupt requests are prioritized first by interrupt request level, then by slot position. Level 7 interrupt requests are the highest priority and level 1 is the lowest. Equal interrupt request levels are serviced in the slot prioritized order A0, A1, B0, ... D1, E0, E1. For more details regarding interrupt prioritization, see Chapter 2.

Table B-4 Interrupt Level Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	0	IRQ 1 IL2	IRQ 1 IL1	IRQ 1 IL0	0	IRQ 0 IL2	IRQ 0 IL1	IRQ 0 IL0
R/W	Reads '1's Writes discarded	Read '0' Writes discarded	R/W	R/W	R/W	Read '0' Writes discarded	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: IRQN IL2-IL0: The interrupt level bits for IRQN.

B.5.4 General Purpose Registers A to E (600/601 to 608/609)

General purpose registers A to E are completely user definable. These read/write registers can be used for semaphores, shared memory, etc. For more application information regarding these registers, see Appendix D.

Table B-5 General Purpose Register Bit Description

Bit #	B15-B8	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	Not Used	GPR7	GPR6	GPR5	GPR4	GPR3	GPR2	GPR1	GPR0
R/W	Reads '1's Writes discarded	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-up State		0	0	0	0	0	0	0	0

NOTE: GPR7-GPR0: The General Purpose Register byte value.

B.6 VMESC5 Programming Examples

The following examples illustrate how to program the VMESC5 to achieve various operational modes.

B.6.1 Reset Example

This example resets one, then all five IP Modules, and then monitors the reset signals to determine when they are de-asserted. Setting a bit in the reset register causes a one-shot to assert the corresponding IP Module reset signal (the one-shot asserts the reset signal for approximately 240 ms). The reset signal can then be monitored by reading the Reset register to determine when it is de-asserted.

- Write '0001' *hex* to the Reset register. This resets the IP Module in slot A by asserting the IP Module A reset signal.

LOOP1:

- Read the Reset register.
- If Bit 0 is set then go to LOOP1.
- Write '001F' *hex* to the Reset register. This resets all five IP Module modules by asserting their corresponding reset signals.

LOOP2:

- Read the Reset register.
- If any of bits [4:0] are set then go to LOOP2.

B.6.2 Interrupt Initialization Example

Interrupts in the VME system are prioritized in a two tier fashion:

- The first tier of prioritization is the interrupt request level, with level 7 being the highest priority and level 1 the lowest.
- The second tier of prioritization is determined by the relative position in the interrupt daisy chain.

The closer the interrupt requester is to the interrupt handler in the daisy chain, the higher its priority for a given request level. The relative position in the daisy chain is determined by the VME chassis slot location and the IP Module slot location on the VMESC5 carrier. The VMESC5 IP Module slot priority order from highest to lowest is A0, A1, B0, ... D1, E0, E1. For more details regarding interrupt prioritization, see Chapter 2. or Appendix D. The following examples illustrate several interrupt service priority schemes.

EXAMPLE 1

In this example, all interrupters are set to the same interrupt request level.

- Write '0011' *hex* to Interrupt Level register A
- Write '0011' *hex* to Interrupt Level register B
- Write '0011' *hex* to Interrupt Level register C
- Write '0011' *hex* to Interrupt Level register D
- Write '0011' *hex* to Interrupt Level register E

Now all ten interrupt sources are set to interrupt request level 1. If all ten sources assert an interrupt request at the same time, they will be serviced in the following order: A0, A1, B0, B1, C0, C1, D0, D1, E0, E1.

EXAMPLE 2

In this example, the interrupt request levels are set to different values to illustrate that the interrupt-request-level prioritization takes precedence over the slot prioritization.

- Write '0011' *hex* to Interrupt Level register A
- Write '0022' *hex* to Interrupt Level register B
- Write '0032' *hex* to Interrupt Level register C
- Write '0054' *hex* to Interrupt Level register D
- Write '0076' *hex* to Interrupt Level register E

For this configuration, if all ten sources assert an interrupt request at the same time, they will be serviced in the following order: E1, E0, D1, D0, C1, B0, B1, C0, A0, A1.

NOTE: It is not normally possible to assert simultaneous interrupt requests, except via special IP Modules like the Systran TESTIP.

APPENDIX C
PERFORMANCE

TABLE OF CONTENTS

FIGURES

C.1 Overview

This section provides several sets of empirical data that present typical performance parameters beyond those provided in the specification. The important feature is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in Chapter 2. and Appendix A.

C.2 State Timing Diagrams

The VMESC5 test configuration consisted of a typical VME card cage with a MVME-162-23 as the host CPU and one Systran TESTIP installed in slot 'A' (refer to Figure C-1for the performance test equipment configuration). For Figures C-2 through C-10 the state waveforms were made using the HP 1 GHz Timing Master Module and the Systran IP Module Logic Bus Extender (IPLBE) with the IP Module Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer's screen are active low, and are represented by a 'V_' or a 'N_' as the first characters to indicate active low signals.

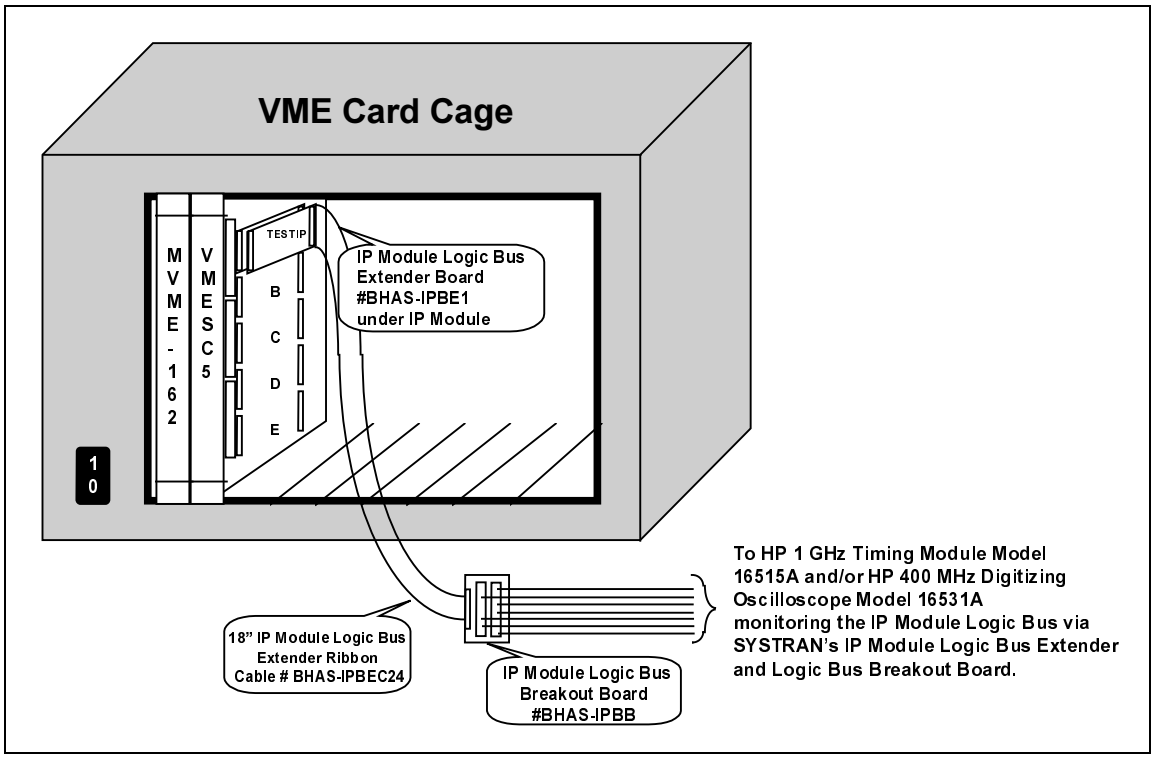

Figure C-1 Performance Test Equipment Configuration

C.2.1 ID Read Cycle

Figure C-2 is a complete ID read cycle of the TESTIP on the VMESC5 in slot 'A'. On the left side of the figure the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IP Module read cycle by asserting the ID_SEL signal. The VMESC5 always begins an IP Module select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IP Module terminate cycle. On the right side of the figure the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME Read cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME read cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME read cycle is complete in three IP Module (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

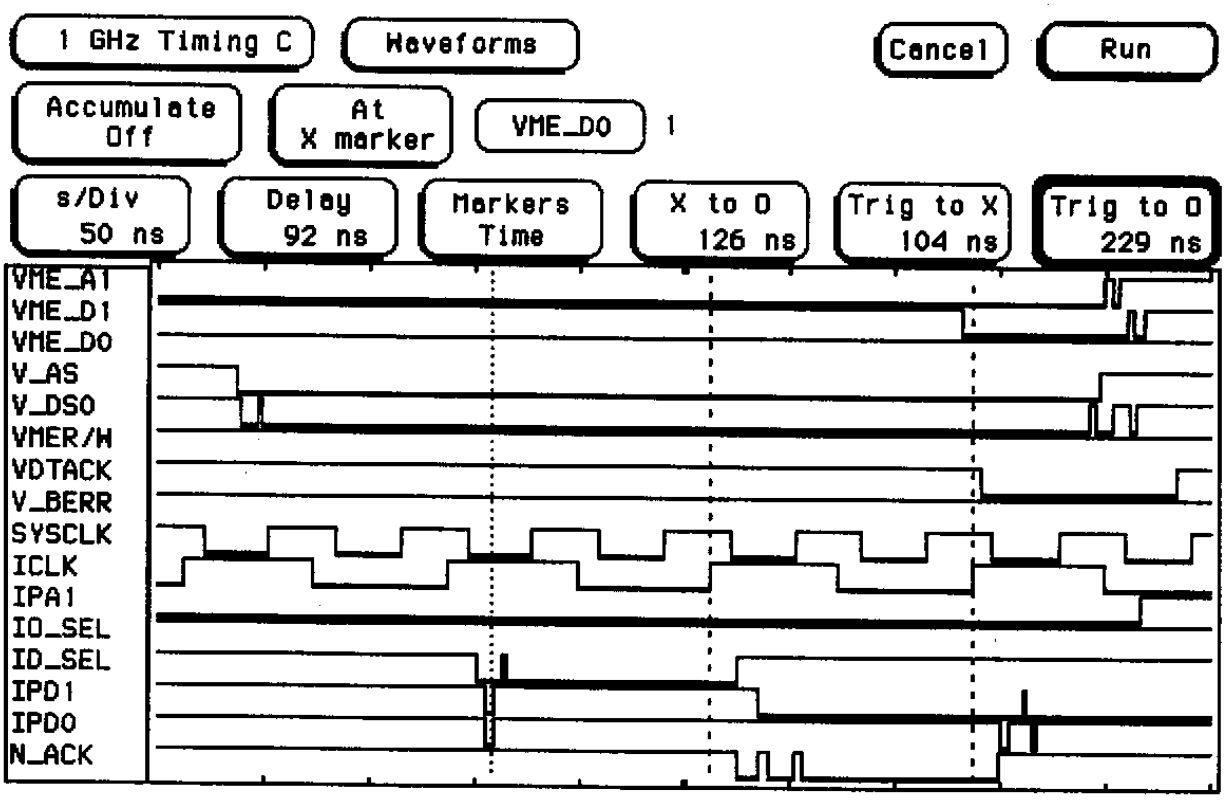

Figure C-2 ID Read

C.2.2 I/O Read Cycle

Figure C-3 is a complete I/O read cycle of the TESTIP on the VMESC5 in slot 'A', which is functionally the same as the ID read cycle. On the left side of the figure, the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IP Module read cycle by asserting the IO_SEL signal. The VMESC5 always begins an IP Module select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IP Module terminate cycle. On the right side of the figure, the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME read cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME read cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME read cycle is complete in three IP Module (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

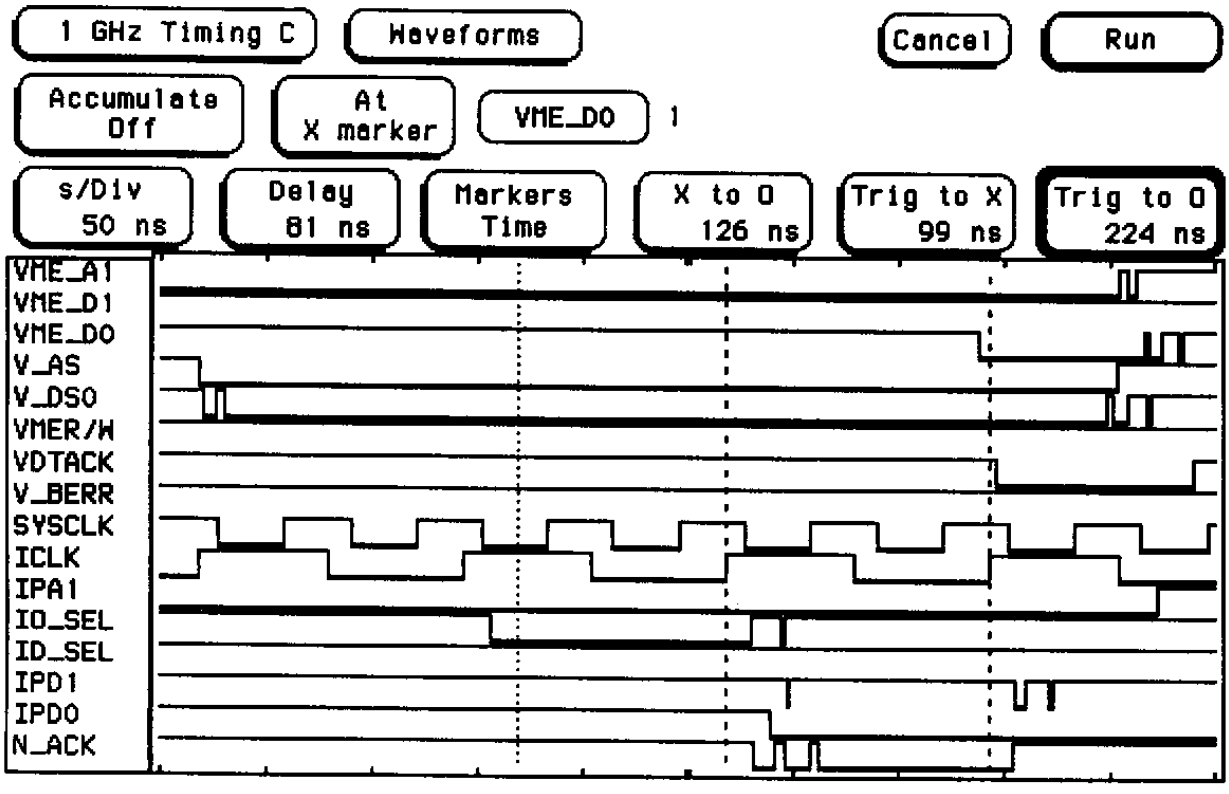

Figure C-3 I/O Read

C.2.3 I/O Write Cycle

Figure C-4 is a complete I/O write cycle to the TESTIP on the VMESC5 in slot ‘A’ . On the left side of the figure, the MVME-162 initiated a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal, and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, in the center of the figure, the VMESC5 DTE begins an IP Module write cycle by asserting the IO_SEL signal and driving the IP Module data bus with VMEbus data. Again, the VMESC5 begins an IP Module select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP asserts the N_ACK signal to complete the IP Module terminate cycle and latches the data from the VMEbus on the rising edge of ICLK (at the end of the terminate cycle). About 9 or 10 nanoseconds after the TESTIP latched the data, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME write cycle by de-asserting the address and data strobes signals. After the VME host CPU terminates the VME write cycle the VMESC5 de-asserts the VDTACK signal. The entire VME write cycle is complete in three IP Module (8 MHz) clock cycles (which is 375 ns). The VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5’s average 375 ns. Although not shown, the ID WRITE cycle is functionally the same as the I/O WRITE cycle. The only difference is that the ID_SEL is asserted rather than the IO_SEL line.

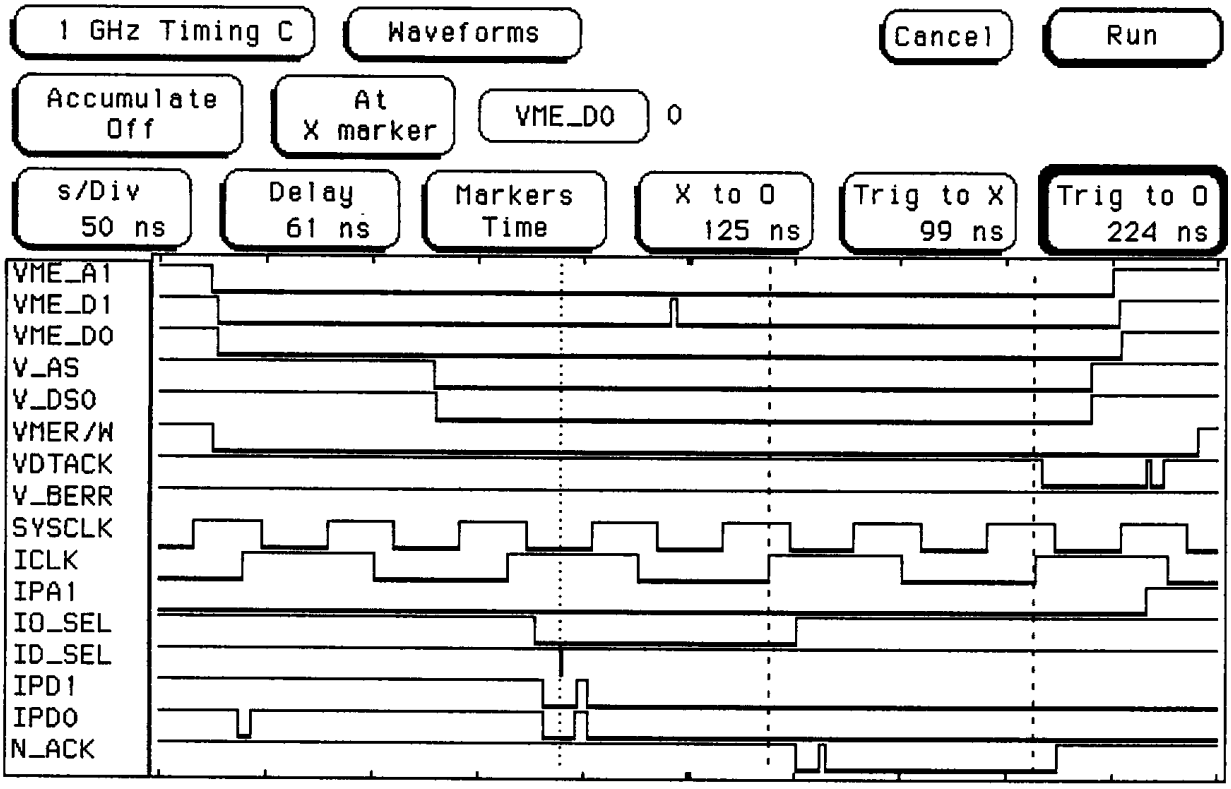

Figure C-4 I/O Write

C.2.4 I/O Read-Modify-Write Cycle

Figure C-5 is a complete I/O read-modify-write cycle to the TESTIP on the VMESC5 in slot 'A'. On the left side of the figure, the MVME-162 initiated a VME read cycle by asserting a valid address and then asserting the VME address and data strobe (V_AS and V_DS0) signals. The read cycle completes as in Figure C-3 and then in the center of the Figure C-5, the VME host CPU de-asserts the data strobe signal while keeping the address strobe asserted. A few clock cycles later, the host CPU begins a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal and then re-asserting the VME data strobe (V_DS0) signal. On the right side of Figure C-5, the write cycle terminates normally as in Figure C-4, completing the VME read-modify-write cycle. Notice that the complete read-modify-write cycle was executed by the host CPU in approximately 1.4 μs.

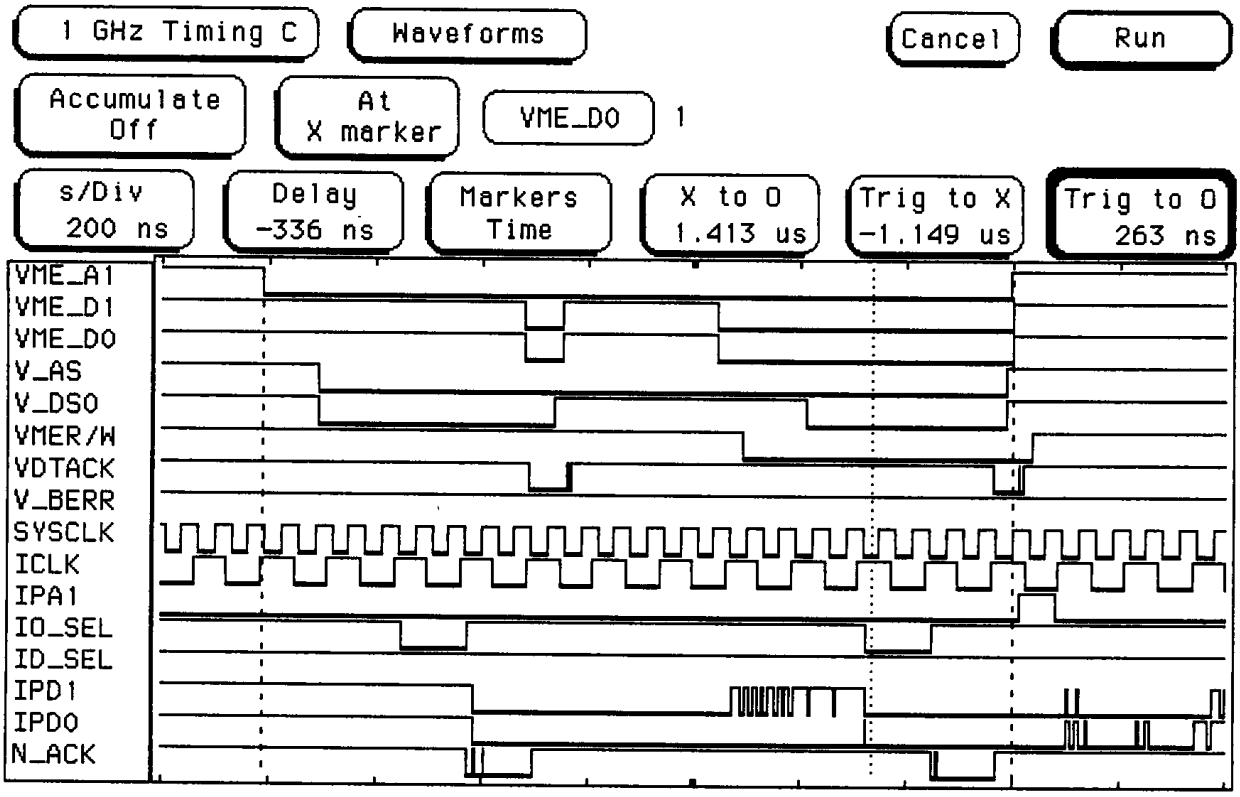

Figure C-5 Read-Modify-Write

C.2.5 I/O Write Cycle With IP Module Wait States

Figure C-6 is a complete I/O write cycle to the TESTIP on the VMESC5 in slot 'A', similar to Figure C-4 except with IP Module wait states inserted. On the left side of the figure the MVME-162 initiated a VME write cycle by asserting a valid address and data along with the VME write (VMER/W) signal and then asserting the VME address and data strobe (V_AS and V_DS0) signals. Next, the VMESC5 DTE begins an IP Module write cycle by asserting the IO_SEL signal. In the center of the figure, the TESTIP has inserted five IP Module wait states then asserts the N_ACK signal to complete the IP Module terminate cycle. Then on the right side of the figure, the write cycle terminates normally as in Figure C-4 completing the VME write cycle with wait states. Note, the VMESC5 will support ID, IO, and Interrupt IP Module cycles with wait states inserted.

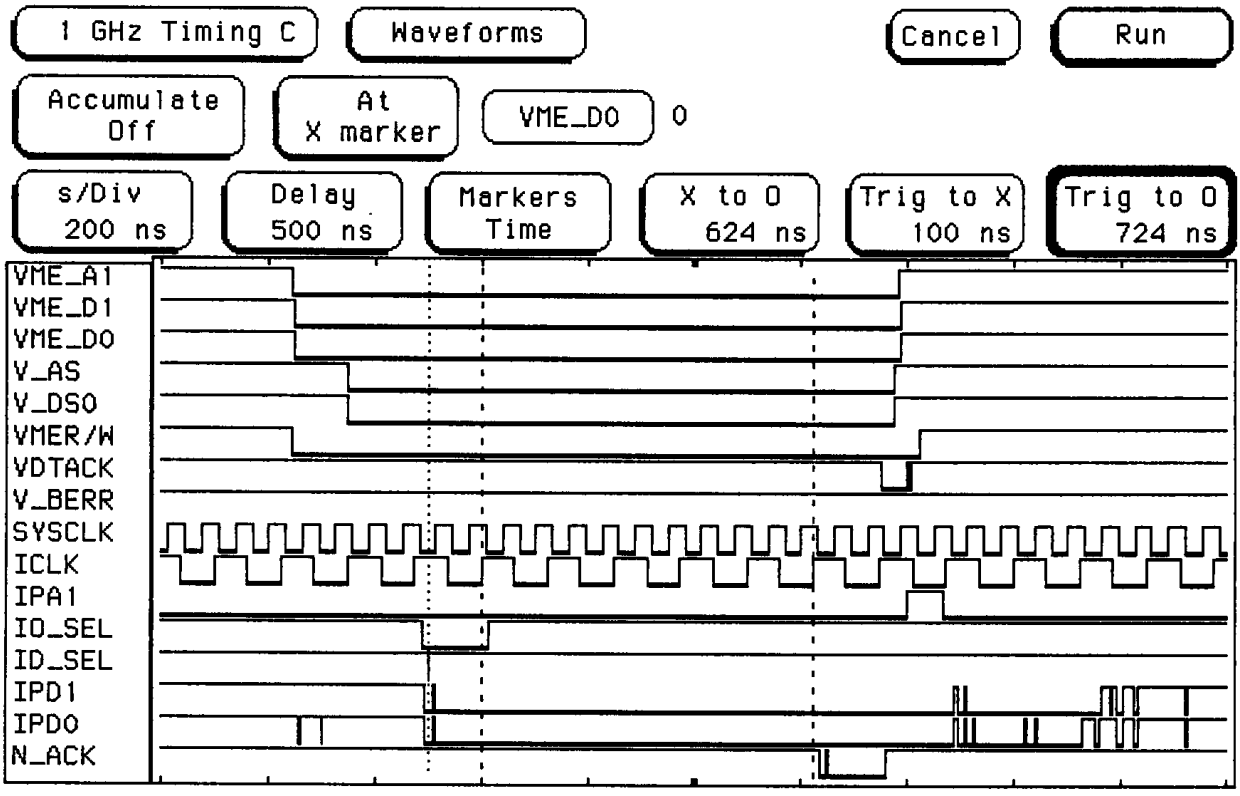

Figure C-6 I/O Write With Wait States

C.2.6 Interrupt Request

Figure C-7 is a waveform view of a complete interrupt request from the TESTIP and the following interrupt service routing (ISR) from the MVME-162 host CPU. For this test, the VMESC5 was configured to drive the VME interrupt level one request (V_IRQ1) when the TESTIP asserted the IP Module interrupt request signal zero (INTRQ0). On the left side of the figure, the TESTIP has asserted the INTRQ0 and about 1.5 µs later the host CPU began the ISR with an interrupt acknowledge cycle fetching the interrupt vector from the TESTIP. In the center of the figure, the host CPU reads a status register on the TESTIP and then on the right side of the figure, the host CPU terminates the interrupt request and the end of the ISR. Figures C-8 and C-9 show more detail timing data of the VMESC5 interrupt cycles.

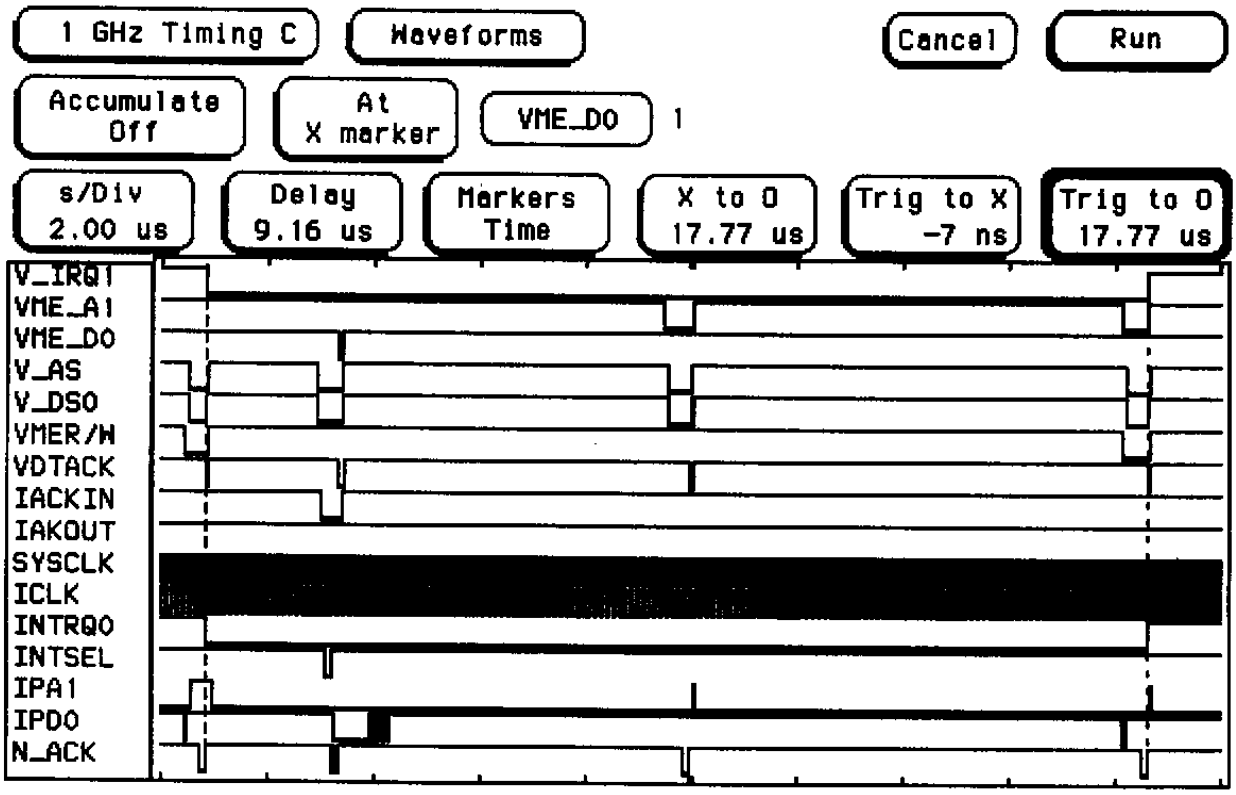

Figure C-7 Complete Interrupt Request and Service Routine

Figure C-8 is a zoomed in view of the TESTIP driving the INTRQ0 signal and in turn the VMESC5 driving the VME interrupt request level one signal (V_IRQ1) in about 14 ns.

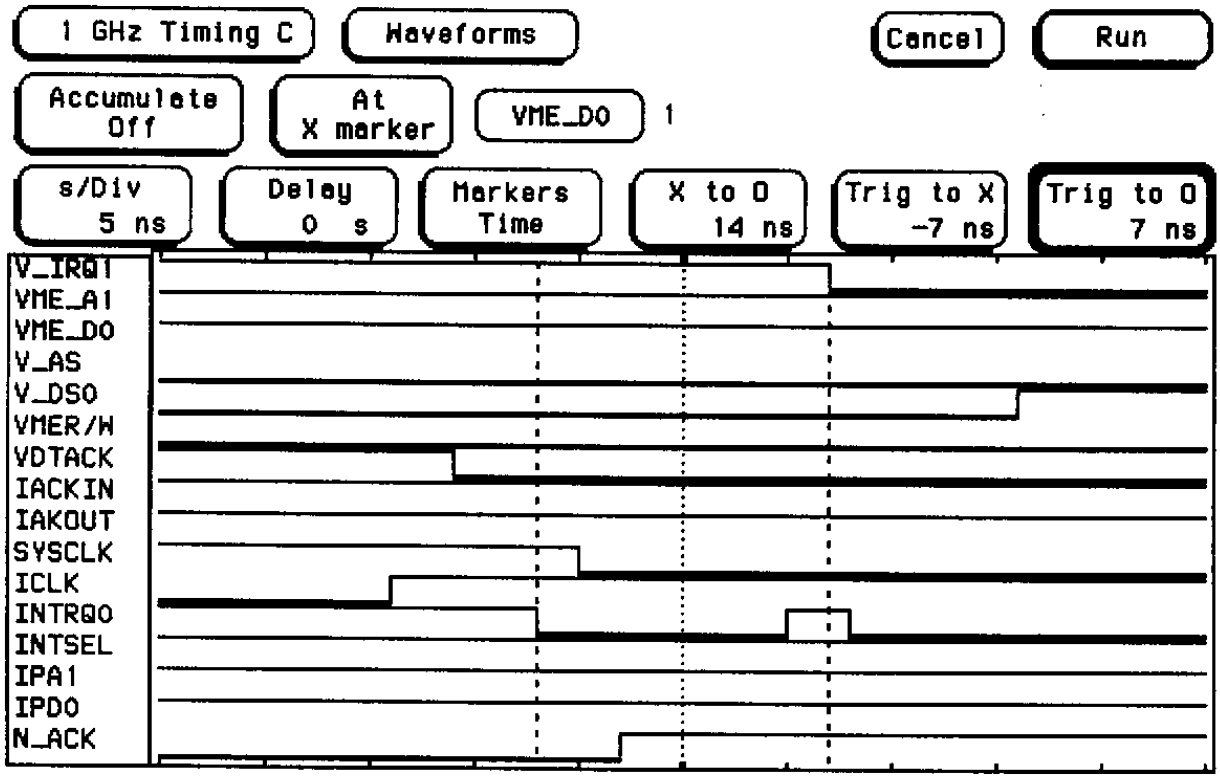

Figure C-8 IP Module INTREQ0 Driving VME IRQ1

Figure C-9 is a zoomed in view of the TESTIP placing an interrupt vector onto the VME data bus. This interrupt vector cycle functions the same as the ID and IO read cycles. On the left side of the figure, the MVME-162 initiated an interrupt acknowledge cycle by asserting a valid address (for the interrupt level being serviced) and then asserting the VME address, data strobe, and interrupt acknowledge input (V_AS, V_DS0, and IACKIN) signals. Next in the center of the figure, the VMESC5 interrupt engine determines if this interrupt acknowledge cycle is for this IP Module and of so begins an IP Module interrupt cycle by asserting the INTSEL signal. The VMESC5 always begins an IP Module select cycle within one ICLK cycle of detecting a valid VME access. In the very next ICLK period, the TESTIP begins driving the data bus and asserts the N_ACK signal to complete the IP Module terminate cycle. On the right side of the figure, the VMESC5 DTE latches the data from the TESTIP on the rising edge of ICLK (at the end of the terminate cycle) and drives the VME data bus. About 9 or 10 nanoseconds after the VME data bus is driven, the VMESC5 asserts the VME data acknowledge (VDTACK) signal and waits for the VME host CPU to terminate the VME interrupt acknowledge cycle by de-asserting the address and data strobes, and IACKIN signals. After the VME host CPU terminates the VME interrupt acknowledge cycle, the VMESC5 releases the data bus and de-asserts the VDTACK signal. The entire VME interrupt acknowledge cycle is complete in three IP Module (8 MHz) clock cycles (which is 375 ns). Again the VMESC5 worst and best case access times are plus or minus one 16 MHz VME SYSCLOCK (± 62 ns) from the VMESC5's average 375 ns.

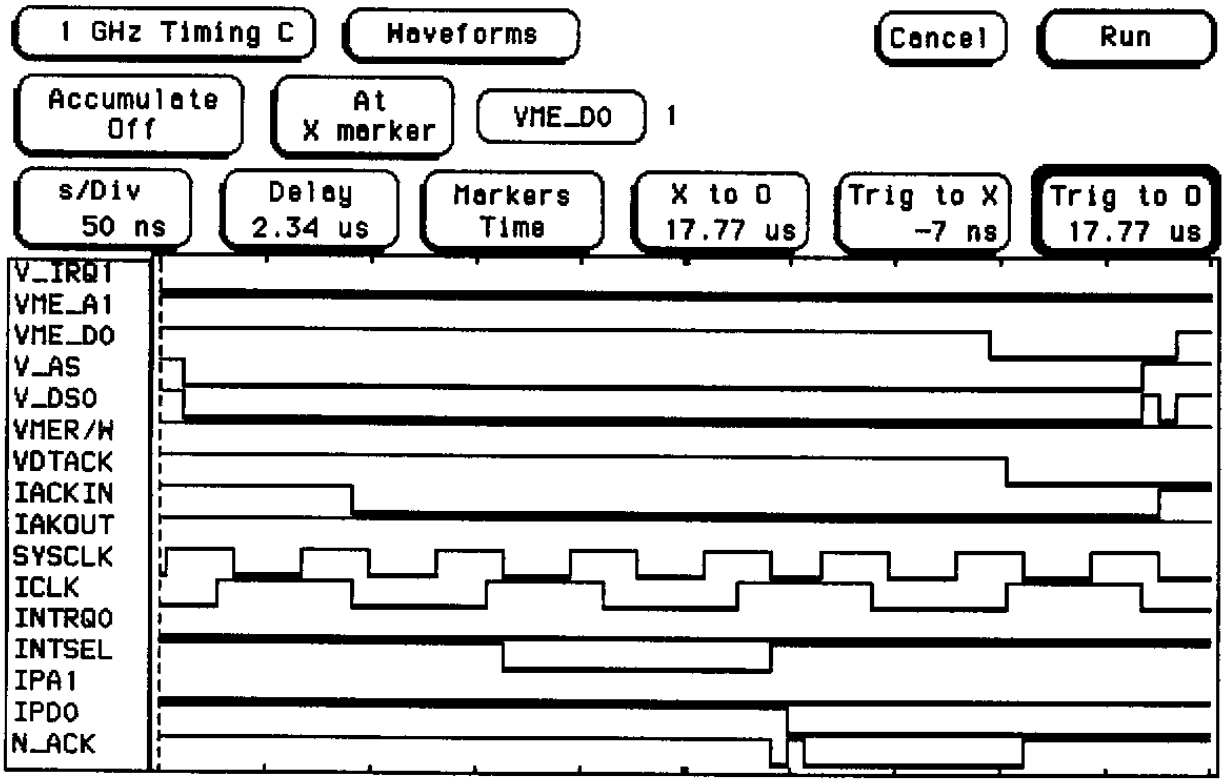

Figure C-9 IP Module Interrupt Vector Cycle

Figure C-10 is a zoomed in view of the VMESC5 driving the VME IACKOUT (IACKIN on the waveform screen) signal in about 64 ns. In this figure, the VMESC5 interrupt engine determined that this interrupt acknowledge cycle was not for any of its IP Modules and very quickly passed on the IACKOUT signal in the VME daisy-chain.

NOTE: Figure C-10 is very important information for users concerned about system response time with the VME IACKOUT daisy-chain signal being passed along by the VMESC5 in about 64 nanoseconds. This means that the VMESC5 will not cause a VME system time-out or bus error by driving the IACKOUT signal as fast as possible. If a VME card cage had one host CPU (VME bus master) and twenty VMESC5 IP Module carriers installed, the last VMESC5 (furthest from the host CPU) with an IP Module in slot 'E' will see the IACKIN signal in about 1.3 µs.

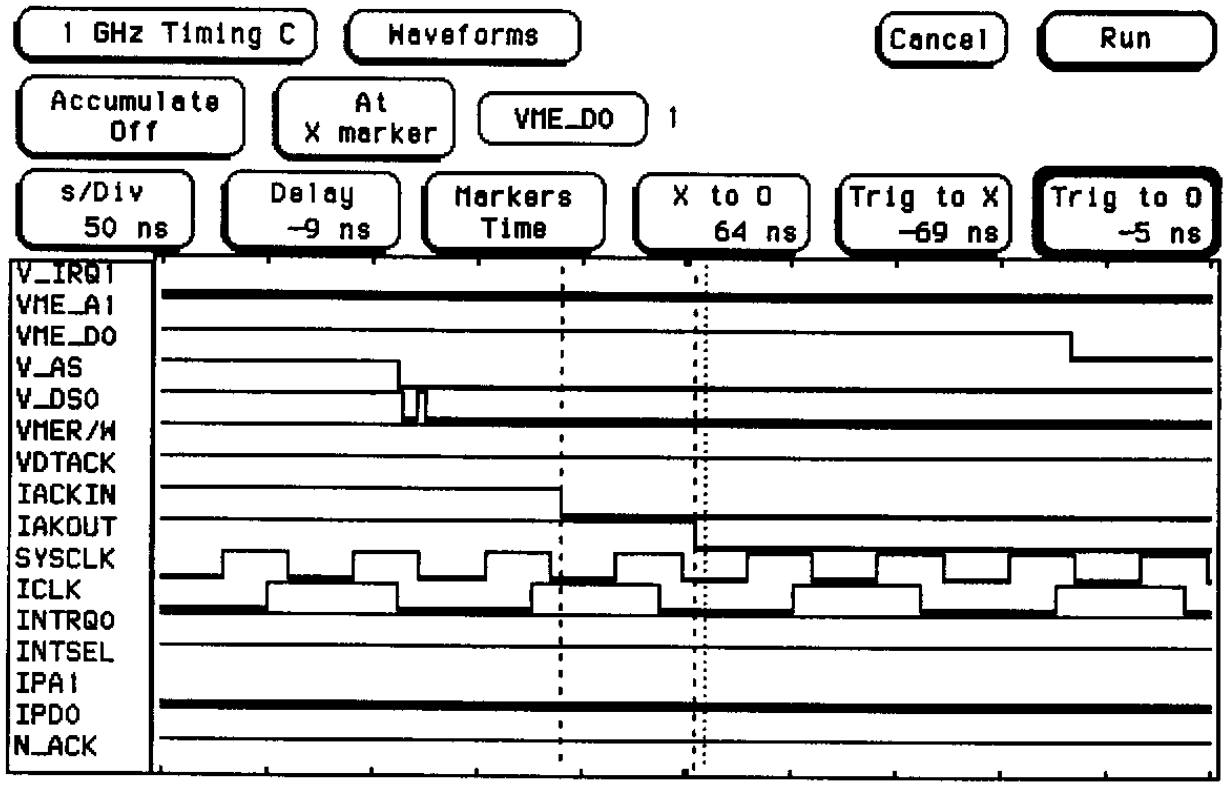

Figure C-10 VME IACKIN to IACKOUT

APPENDIX D
TYPICAL APPLICATIONS

TABLE OF CONTENTS

FIGURES

D.1 Applications

Systran Corp. extends an open invitation to all users to freely submit their applications that might, or do, use the VMESC5 Slave Carrier to solve a problem. This section of the manual will be revised periodically to include new application ideas for all users to consider. Help advance the level of technology by participating with the Systran team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and Systran Corp. reserves the right to modify submissions to provide for more generic appeal, when necessary.

D.2 Sharing IP Modules between Multiple VME Masters

It is sometimes desirable for multiple VME bus masters to share IP Module resources. In this case, a semaphore is typically used to lock out access to the resource when it is in use. This example illustrates using the General Purpose registers on the VMESC5 for this purpose.

Figure D-1 depicts a system that is comprised of two VME masters, and one or more VMESC5 carriers populated with I/O modules, in a process monitor and control application. In this hypothetical system, one master performs the process control functions while the second master monitors all of the I/O data values and reports the

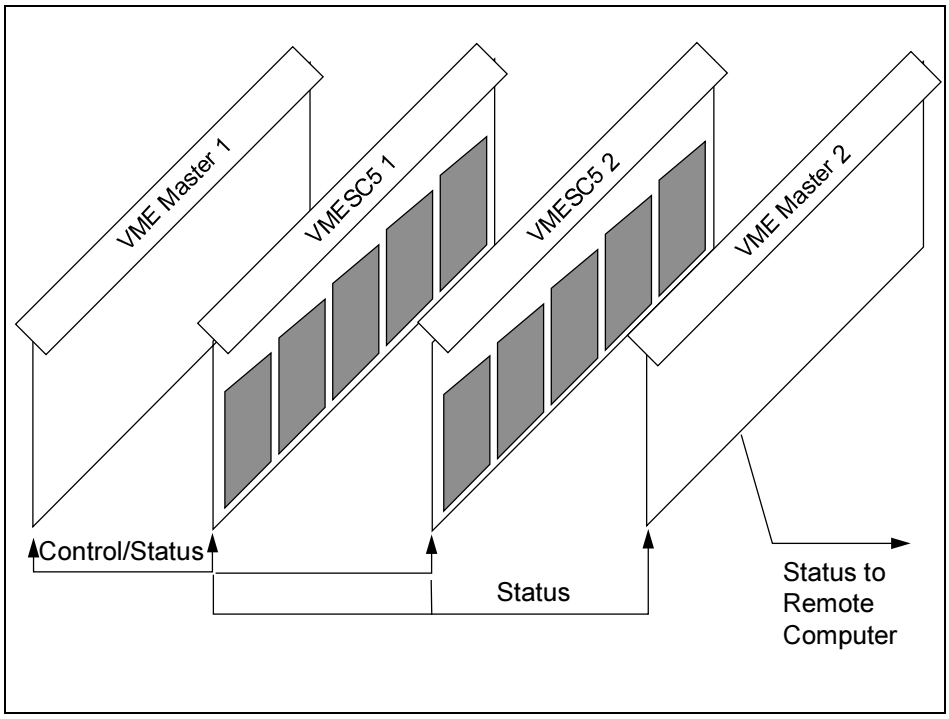

Figure D-1 A System With Two VME Masters

information to a remote computer. The second master is presumably used because one master cannot handle both the process control and communication functions.

The data being reported to the remote computer from any one IP Module must be from the same frame. To insure this requirement is met, a separate semaphore is used for each

IP Module. The exchange of data between the VME masters and the IP Modules would then go something like this, where "x" is the last IP Module on the last carrier:

D.2.1 VME Master 1

- Reserve IP Module A semaphore (in General Purpose register A). If not available then wait until it is available.
- Set the new output values for IP Module A.
- Release IP Module A semaphore.
    -
    -
    -
- Reserve IP Module x semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Set the new output values for IP Module x.
- Release IP Module x semaphore.

D.2.2 VME Master 2

- Reserve IP Module A semaphore (in General Purpose register A). If not available then wait until it is available.
- Read the data from IP Module A.
- Release IP Module A semaphore.
- Send the IP Module A data to the remote computer.
    -
    -
    -
- Reserve IP Module x semaphore (in corresponding General Purpose register). If not available then wait until it is available.
- Read the data from IP Module x.
- Release IP Module x semaphore.
- Send the IP Module x data to the remote computer.

This is just one example of using the General Purpose registers. They are completely user definable and therefore can be used for any purpose.

D.3 Configuring Interrupts for Multiple Priority Schemes

Some systems must run more than one application for a given hardware configuration. The two applications may require two distinct interrupt priority schemes. This example illustrates how to configure the interrupt level registers on the VMESC5 to achieve two different priority schemes.

The following assumptions are used for this example:

1. The two applications each use five IP Modules, A through E.
2. Each IP Module utilizes interrupts IRQ0 and IRQ1.
3. Application one requires that the interrupts be serviced in the following order:
   C0, C1, B0, B1, A0, A1, D1, D0, E0, E1.
4. Application two requires that the interrupts be serviced in the following order:
   D1, E1, D0, E0, C0, C1, A0, A1, B0, B1.
5. Interrupt level 7 should not be used.

Recall that the IACK daisy chain slot priority is:
A0, A1, B0, B1, C0, C1, D0, D1, E0, E1
which represents the servicing order for equal level interrupt requests. Therefore, the solution is to set interrupt request levels to override the slot priority, where necessary, to achieve the desired servicing order.

To achieve the desired servicing order for application one, the interrupt levels could be set as follows:

- Write ‘0033’ *hex* to Interrupt Level register A
- Write ‘0044’ *hex* to Interrupt Level register B
- Write ‘0055’ *hex* to Interrupt Level register C
- Write ‘0032’ *hex* to Interrupt Level register D
- Write ‘0022’ *hex* to Interrupt Level register E

To achieve the desired servicing order for application two, the interrupt levels could be set as follows:

- Write ‘0022’ *hex* to Interrupt Level register A
- Write ‘0022’ *hex* to Interrupt Level register B
- Write ‘0033’ *hex* to Interrupt Level register C
- Write ‘0054’ *hex* to Interrupt Level register D
- Write ‘0054’ *hex* to Interrupt Level register E

In both cases, there is more than one possible combination of Interrupt Level register settings that could be used to produce the desired results.

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GLOSSARY

[x:y]---------- Nomenclature designating a bit-range, where "x" is the left-most bit and "y" is the right-most bit. (e.g. Data bus [7:0] refers to the least significant eight bits).

aperture ---------- A region or set of addresses.

byte-lane ---------- Eight bits of a data bus on octal boundaries.

CSR---------- Control and Status Register.

doublewide ---------- An IP Module that is twice the size of the singlewide board.

EPLD ---------- Erasable Programmable Logic Device.

IP Module---------- Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.

IP Module logic bus---------- A synchronous, 4 MTransfers/sec, 16-bit wide bus that includes I/O, memory, ID PROM, and interrupts. The address bus is 6-bits wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.

ISR---------- Interrupt Service Routine, Interrupt Status Register, or Interrupt Steering Register

MTBF---------- Mean Time Between Failures.

ns, μs, ms---------- Nanoseconds, microseconds, and milliseconds respectively.

singlewide---------- An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.

VHDL---------- Very high-speed integrated circuit Hardware Description Language.

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