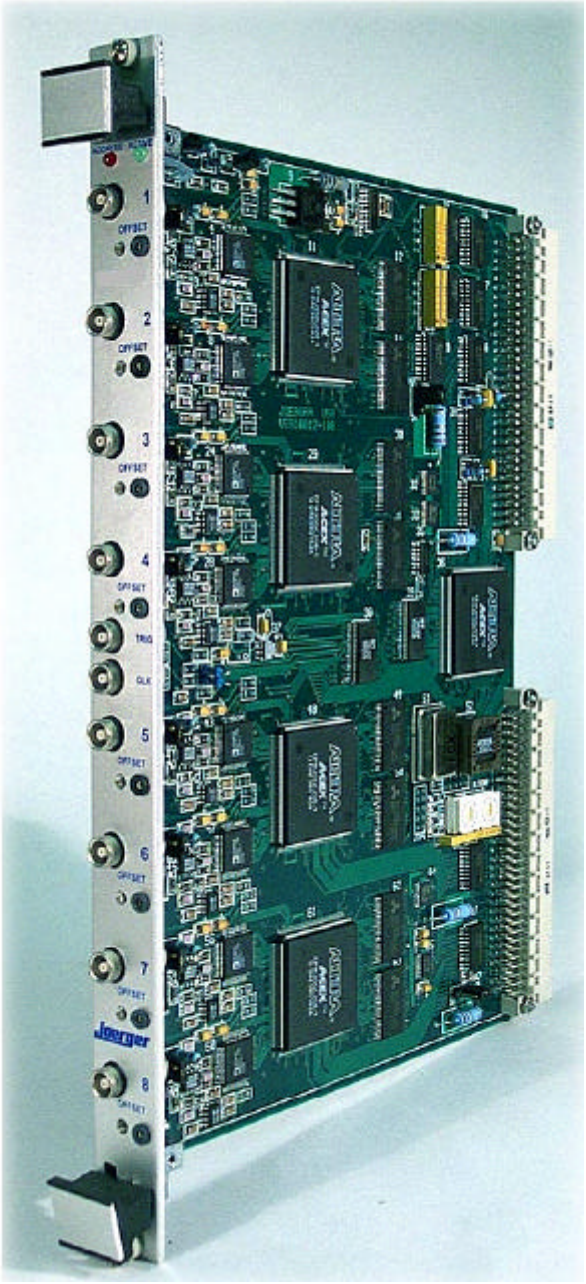
Joerger ENTERPRISES, INC.

MODEL VTR8014

EIGHT CHANNEL, 80 MHZ, 14 BIT "VME" ANALOG DIGITIZER WITH OSCILLOSCOPE CHARACTERISTICS

FEATURES:



- EIGHT INDIVIDUAL CHANNELS
- 80 MHZ CLOCK SPEED
- 14 BIT RESOLUTION PLUS SIGNAL AVERAGING FOR IMPROVED SNR
- ***"OSCILLOSCOPE"*** TYPE INPUTS FEATURING:
  - HIGH INPUT IMPEDANCE, 10 MΩ's
  - FULL SCALE OFFSET CONTROL
  - SINGLE ENDED OR DIFFERENTIAL INPUTS
  - WIDE INPUT BANDWIDTH FOR GOOD WAVEFORM TRACKING
- 256K SAMPLES OF SRAM PER CHANNEL, 2M SAMPLES TOTAL
- CHANNELS CAN BE READ AT ANY TIME PROVIDING:
  - SIGNAL MONITORING
  - OFFSET ADJUSTMENT
  - GAIN TESTING
- RECORDING MODES:
  - POST TRIGGER
  - MULTIPLE POST TRIGGER
  - PRE/POST TRIGGER
  - MULTIPLE PRE/POST TRIGGER
- GLOBAL COMMANDS FOR MULTIPLE MODULE OPERATION
- ALL TRIGGER ADDRESSES STORED
- REAL TIME TRIGGER ARRIVAL STORED
- TRIGGER COUNTER PROVIDED
- NUMBER OF EVENTS REGISTER
- INDIVIDUAL FILTERING OF EACH CHANNELS POWER AND GROUND
- HIGH NOISE IMMUNITY AND LOW CHANNEL CROSSTALK
- ***"SPARSE"*** SCAN MODE FOR IMPROVED READOUT SPEED

- LOW POWER CONSUMPTION, 18 WATTS TOTAL AT 80MHZ, GREATLY IMPROVING CRATE COOLING AND MODULE RELIABILITY
- 64 BIT DATA READOUT AVAILABLE USING MBLT64, 4 DATA WORDS PER READ
- ACTIVE MODE CAN BE DELAYED FROM TRIGGER SIGNAL, PROGRAMMABLE
- INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE
- ***"EPICS "*** SOFTWARE AVAILABLE

APPLICATIONS:

- HIGH SPEED, ACCURATE, ANALOG CONVERSION
- ***OSCILLOSCOPES:*** USING ITS HIGH IMPEDANCE FRONT END, FULL SCALE OFFSET AND MEMORY PROVIDE FAST, ACCURATE RECORDING AND READOUT OF ANALOG DATA, ESPECIALLY USEFUL IN SINGLE SHOT EVENTS
- COMMUNICATIONS: USING THE REAL TIME ADC OUTPUT
- RADAR AND SATELLITE SYSTEMS

The ***JOERGER ENTERPRISES, INC.*** MODEL VTR8014 contains eight, 80Mhz analog digitizers with a resolution of 14 bits plus signal averaging for improved SNR in a 6U, VME module. In addition to waveform recording the input has the same features as an oscilloscope, 10MΩ input impedance, full scale offset and single ended or differential inputs. This provides the ability to record a single shot event with high speed and resolution and read it out quickly. This simplifies system analysis and trouble shooting. High resolution and accuracy have been attained with the use of ADC's designed to run at 80Mhz with 14 bit resolution. To further improve performance the input signals can be averaged to improve signal to noise response. From 2 to 128 input samples can be selected for averaging and the results stored in memory. Each channel is completely self contained and can store up to 256k samples per channel in SRAM, 2M total in a single width module. The latest ADC's, amplifiers, memory and the use of high speed programmable logic devices make all these features possible. While many high speed modules require a great deal of power, the VTR8014 uses only 18 watts while running at 80Mhz. This is often an important consideration when many of these may be used in a single crate. The ADC uses a pipeline converter with the delay handled internally and is invisible to the user.

To insure high performance each channel contains a wide bandwidth amplifier section. To provide good ADC performance it is driven with a buffered amplifier with a differential input and a differential output which is internally offset to provide an input designed especially for these latest type converters. This isolates the ADC and provides a 10MΩ input impedance with either a single ended or a true differential input. The high input impedance affords the ability to monitor an input signal without loading it down. This type input coupled with its large memory provides the ability to monitor a wave shape over a long period of time. Even when trouble shooting a slow speed system it provides a high speed, high-resolution picture. A difficult feature to accomplish with an analog oscilloscope. When required a lower input impedance can be selected with an on board jumper.

To provide a versatile input range full scale offset is provided using a front panel potentiometer. This allows either bipolar or unipolar input ranges. A test point is included to monitor the offset. The offset can be readout on the VME bus. To make the module even more useful data may be read out while active or idle without disrupting the operation. This allows the data from the ADC to be monitored while active. It provides the ability to operate the module as an ADC or to check each channel's offset and gain.

The input is digitized using an internal crystal oscillator or an external clock and loads the data into its internal SRAM. To insure high-speed readout, data can be read out 4 samples at a time from 2 channels using BLT64 onto 64 lines. To increase overall data readout speed a "SPARSE" scan mode is provided. Each channel has a 14 bit register that can be set with a minimum input level. Its output is compared to the converted input level and if it is not exceeded the data is considered invalid. This valid data word can be read out indicating which channels should be read. All channels use a common clock, address, control signals and operate simultaneously. Special care has been extended to insure accurate timing.

The analog inputs have been designed to handle a wide variety of signals. Each channels analog power and analog ground are individually filtered. This special care in the layout and filtering provide both low channel cross talk and low noise, often a problem with multi-channel analog input modules. When an application requires filtering, external filters are recommended.

Control and status registers are accessed via short addressing. The control registers select the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger.

To facilitate data readout two additional memories are provided. One records the memory address at the end of each cycle. The second memory records the time each trigger was received and is taken from the 32 bit real time counter. A trigger counter is provided to record the number of complete triggers received. This information allows the user the ability to know how many triggers were received, their memory addresses and the time the triggers occurred. An event register is also provided that selects the number of triggers to accept and disarm the cycle.

The Model VTR8014 can operate in post trigger, multiple post trigger, pre/post and multiple pre/post trigger modes. The post trigger mode starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register then stops and sets an interrupt. If Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. For multiple post trigger operation, Auto Reset is turned off and each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. To account for the timing in multiple trigger operations a 32 bit “real time” counter is provided. The time each trigger is received is stored in memory. This can be readout along with the number of triggers received. If the "Memory Wrap" is off and the cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on, when the memory fills it will start overwriting data and accept triggers until the module is disarmed.

In the pre/post trigger mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the gate duration register, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pre-trigger information. For multiple pre/post trigger operation the memory is divided programmably into sections of up to 16. Now each section operates as a pre/post trigger cycle with its address and time stored. At the completion of operation an interrupt is set. This then provides the user a complete picture of the data recorded. The memory addresses, the time the triggers were received and the number of triggers are available. All recording cycles are triggered, either internally or externally. As an added feature this trigger can be delayed digitally by programmable setting of a counter and its clock speed. This could prove useful in operations where there is a time gap when the trigger appears and active recording should begin. In pre/post modes a register is provided to require to set a number of samples to be stored after arm before a trigger is recognized.

To control multiple module operation global commands are available that can be used for commands like arm/disarm, and to enable/disable triggers. This allows the user the ability to control a group of modules and have them work together.

SPECIFICATIONS (per channel)

ANALOG INPUT	±1.1 Volts, single ended, Differential input optional
INPUT OFFSET ADJUST	Full scale front panel input offset adjustment and test point
INPUT IMPEDANCE	10 MΩ's, jumper selectable to 50Ω's, other impedance's optional
CHANNEL CROSSTALK	<1 LSB typical at 10Mhz input rate
BANDWIDTH	100Mhz Minimum
DIFFERENTIAL LINEARITY	±.25LSB, Typ., No missing codes
CONVERSION RATE	30Mhz to 80Mhz
RESOLUTION	14 Bits + over-range
SIGNAL AVERAGING	Select number of samples to be averaged, 2, 4, 8, 16, 32, 64, 128
MEMORY	256k samples/channel in SRAM, 2M samples total
TRIGGER/GATE INPUT	TTL Level, Operating mode internally selectable
CLOCK INPUT	TTL Level
VME INTERFACE	D16, D32, D32:BLT, BLT64, A16, A24, A32
CONTROL/STATUS REG.	Read/Write: disarm at cycle completion, bus trigger, external clock, external trigger/gate, reset on trigger, wrap, post, multiple post, pre/post, and multiple pre/post trigger modes, arm, active, channel data addresses, real time trigger addresses, trigger delay, trigger counter, trigger selection register, global arm/enable
GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
REAL TIME ADDRESS	Read real time trigger addresses
TRIGGER DELAY	Read/Write active trigger delay
PRE/POST SELECTION	Read/Write, select number of multiple pre/post cycles
EVENT REGISTER	Read/Write, number of trigger events for interrupt and/or disarm
MIN PRETRIGGER SAMPLE REGISTER	Read/Write, minimum number of samples needed before a trigger will be accepted in pre/post trigger modes
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read/Write IRQ levels
SYSRESET, INT. RESET	Resets module and control register, aborts recording cycle
POWER REQUIREMENTS:	+5V, 3A; -12V, 250ma, 18 watts total at 80Mhz
SIZE:	Single width "VME" 6U card
CONNECTORS:	Lemo ERA 00.250 Lemo ERA 0302, for differential inputs
OPTIONS	1) Differential Inputs 2) SMA connectors

JEI0502

PLEASE NOTE: When choosing an analog input module many factors should be considered. It is recommended reading "SELECTING AN ANALOG INPUT MODULE" on our web site: www.joergerinc.com , under "What's New"

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INTRODUCTION

The Joerger Enterprises, Inc. Model VTR8014 contains eight, complete, 80Mhz, 14 bit digitizers in a single width, 6u VME module each with 256k samples of SRAM per channel. The Model VTR8014 uses extended addressing, A32, for data readout, 2 channel at a time over D0-D31. Data is straight offset binary and read out on data lines D0-D13 for channel 1-4, and D16-D29 for channels 5-8. The over range bit can be selected with on board jumpers and is read out on D14 and D30. MBLT64 readout is also provided. Unused data bits return zero. Data from the memory can only be read out when the module is disarmed.

The module uses ADC's that are 80Mhz with 14 bit resolution. They are driven with dc coupled differential input / output amplifiers. The ADC's are the latest pipeline designs that work best when driven with an offset, differential signal. The amplifier has been designed specifically to drive this type of ADC and offers wide bandwidth and superior signal to noise performance. Because it has a differential input it provides the user the ability to select single ended or differential inputs. To provide amplifier protection and high impedance inputs both the signal and return lines are buffered using wide bandwidth amplifiers. On single ended units the return line is grounded. The signal input impedance is greater than 10MΩ's and can be jumper connected to 50Ω's when the application requires. Other input impedances can be ordered To make the module more useful the input can be offset full scale. The standard input is ± 1.1 volt, this can be adjusted with a front panel pot to a range of 0 to +2.2 volts or –2.2 volts to 0 volts.

A major problem with multi-channel devices is channel cross-talk. The performance of a single channel is important but determining if that performance can be achieved when adjacent channels are active is more important. The VTR8014 analog ground and power lines are separately filtered for each channel. This isolates the channels and improves overall module performance greatly. The analog ground layout for each front end has been designed to improve performance and lower noise pickup. Channel cross-talk is less than 1 LSB. To further improve SNR, signal averaging is provided. From 2 to 128 ADC samples can be averaged and the result stored in memory.

To improve readout speed a "SPARSE" scanning mode is provided. A minimum level is stored in a Comparator Threshold Register for each individual channel, or a single write can store the same value for all 8 channels. When the module is active and taking data, each ADC's 14 bit output is compared with the 14 bit Comparator Threshold Register for that channel. If the minimum level is exceeded, the bit for that channel is set in the 8 bit Valid Data Register.. This register can be read to determine which channels can be skipped during data memory read.

The Model **VTR8014** can operate in Post Trigger, Multiple Post Trigger, Pre/Post Trigger and Multiple Pre/Post Trigger modes. The last memory location address for each event (up to 255 events) is stored in a memory to facilitate data reconstruction after readout. For multiple event operation a 32 bit Real Time Counter is provided. which uses a selectable clock providing up to12.5 ns resolution. Upon receipt of each trigger (up to 255) the Real Time Counter reading is stored in a memory. This provides a picture of when each event was triggered. Additionally each completed event is counted (up to 65535).

For applications that may require the Post Trigger event to be started after the receipt of an external trigger, a 16 bit delay counter is provided.

OPERATION

Several operating modes are possible, each of them defined by setting values into registers. All eight channels operate simultaneously with the same setup parameters. All setup should be done prior to Arm.

READ LAST:

The analog converters are always converting whether the digitizer is armed and active or not. This allows the readout of the last conversion from any channel at any time, (even if the module is active). Similar to a free running ADC with readout 'on the fly'. This can be used to track the inputs for setup, offset adjustment or test without any special setup and without changing any mode the module may already be set to. The channels can even be sampled during an active cycle. This is in addition to the data being written into the onboard memory and does not interfere with normal operation in any way.. See tables for location of Last Conversion Registers. This 'on the fly' readout is available with digitizer armed or unarmed but it can contain large errors due to asynchronous operation of the read cycles verses the digitizer clock. Use for setup/test only. The 'D14' Over range jumper controls all channels for this read mode.

TRIGGER DELAY:

For applications that may require the module trigger to be delayed from the front panel trigger, a trigger delay register is provided. The delay can be up to 65535 sample periods (16 bits). A bit in the Status Register is true if a trigger has been received. See 0x2C.

MINIMUM PRETRIGGER SAMPLES:

In PrePost Trigger modes triggers may be ignored until a preset number of PreTrigger samples have been recorded after Arm. The number can be up to 65535 samples (16 bits). See 0x2A.

REAL TIME COUNTER:

A 32 bit Real Time Counter and a 256x32 memory are available for 'time stamping' the receipt of Triggers. The resolution of the RTC can be selected from 12.5ns. 25ns or 125ns. If the RTC is enabled, each trigger writes the RTC value into memory and increments the Trigger Counter (8bits). See 0x3A-0x3C.

POST TRIGGER MODE: (default mode):

After setup and arming, digitizing begins at the selected clock rate following a trigger and takes the number of samples contained in the Gate Duration Register and loads them in memory. The Auto-Reset bit of the Control Register determines whether the location counter is reset by each trigger.. When the Location Counter is not reset by each trigger, data following successive triggers is stored sequentially in memory until the memory is filled, (Multi Post Trigger cycles). If Auto Reset is on, old data is overwritten by new data each time a trigger is received. Operation is the same if using the External Gate mode.

The Completed Post Trigger Cycles Counter (16 bits) contains the number of complete events, is readable while armed and is automatically cleared with the memory location counter. The Completed Post Trigger Cycles Counter Register stores this counter value at Disarm. This is not the maximum number of events that can be recorded, only the maximum number that can be counted. The Event Register may be used to set an interrupt and/or disarm the digitizer after a number of completed events.

The Wrap bit in the Control Register determines if the digitizer stops at the end of memory or wraps around and begins to overwrite memory starting at location zero. If the Wrap bit is off and the memory has been filled, the module is disarmed and additional triggers are ignored This will occur regardless of the condition of the Disarm at End of Cycle bit. The Wrap bit operates the same in the External Gate mode.

The Disarm at End of Cycle bit determines if the module is disarmed at the end of each event. When the gate time is over, active goes to off, the module is disarmed and will not respond to any further triggers or external gate inputs until it is rearmed.

An interrupt is set either on the end of an event, when the module is disarmed or when the Completed Post Trigger Counter equals the number stored in the Event Register, depending on the Interrupter Setup Register

PRE/POST TRIGGER MODE:

: This mode is setup in the Control Register with the appropriate bits set.. Arming starts the digitizer continuously filling the total memory until a trigger is received, then. the number of samples contained in the Gate Duration Register are stored and the event ends.. This allows the capture of data both before and after a trigger. The Wrap bit must be set to allow the memory to be refilled after the address counter overflows. If the memory should not be overwritten set the Wrap bit to zero. The module will automatically be disarmed at the end even if the bit in the control register is not set.. In addition to triggered operation, this mode can be combined with the External Gate mode allowing capture of data before an external gate. The Pre/Post Trigger bit in the Control Register is cleared on active going to zero. A bit in the Status Register will be set if the memory address counter overflows at least once.

MULTI-PRE/POST TRIGGER MODE:

This mode allows for multiple (the total memory divided into 2, 4, 8 or 16 segments) Pre/Post Trigger cycles to be recorded along with the memory location address of the last sample recorded in each segment. The Completed Post Trigger Cycles Counter stores the number of post trigger cycles completed, can be readout while the module is active and is useable in all modes.. The last address of each completed post trigger cycle is stored in the Last Address Memory.

The mode is set up by writing to the Multiple Pre/Post Setup Register and setting the Gate Duration Register with the number of post trigger samples required. The digitizing is started by arming.. The samples are recorded in the first segment in a circular overwriting manner until a trigger is received. Then the number of post trigger samples selected are taken, the address of the last sample for that segment is stored in the Last Address Memory, and the next segment is automatically started. When the last segment (2, 4, 8 or 16) is completed, the module is disarmed ,the digitizing is stopped and the total memory is filled. The module can also be stopped by disarming it at any time and the Completed Post Trigger Cycle Counter will contain the number of completed segments.

Data readout is organized as follows. The number of segments set, the total module memory size and the channel number determine the lowest and highest VME address for each segment. The address for the last sample of each segment is retrieved by first writing to address (0x34) to reset the readout pointer and then reading from address (0x34) continuously, see tables. This allows readout of the total memory and all the event ending addresses for later organization or readout of specific samples for each segment. While armed, readout of the Completed Post Trigger Cycle Counter will always contain the number of completed post trigger cycles and can be used to check on the progress of the cycles. After disarm the Completed Post Trigger Counter Register should be used since it is valid until the next disarm.

EXTERNAL GATE MODE:

This mode is enabled by setting the Ext Gate Enabled bit in the Control Register and arming the module. Setting this bit automatically changes the function of the Trig/Gate input to the gate function. This allows the front panel input to start (up edge) and stop (down edge) the digitizer. The Disarm at End of Cycle, Wrap, Pre/Post Trigger and Auto Reset bits all work normally and the interrupt is set when the Trig/Gate input goes to zero (active also goes to zero).

RESET:

A complete reset of the module (the same as Sysreset) is done with a VME write cycle to Short Address base +(0x00). This will abort the cycle, clear all setup parameters, clear the internal interrupt latch, take any pending IRQ off the bus and disable the IRQ response. This leaves the VTR8014 in it's power up condition with all registers set to default.

INTERRUPT:

The interrupt is enabled and setup from the Interrupter Setup Register.. When the IRQ is disabled by clearing a bit in this register, the IRQ is removed from the VME bus and the internal IRQ source is cleared.. The status of the internal interrupt may be read from the Status Register, and can be used with the Enable IRQ bit in the setup register at 0. Depending on Interrupter setup, an interrupt is set in any operating mode when a cycle is completed (active goes to zero) or when disarm occurs or when the Completed Post Trigger Counter equals the number stored in the Event Register. The IRQ is reset on acknowledge for an addressed IACK cycle (ROAK), or by Sysreset, Master Reset or Reset IRQ Source (0x16). The byte stored in the Interrupter Status/ID Register is returned with the acknowledge for the IACK cycle.

Power-up and Master Reset:

Set all registers and storage elements to default value. The default value is false (0 or reset) for all except the Front Panel an Software Trigger Enables (Control Register) whose default is true (1 or set).

FRONT PANEL SIGNALS

Analog Input Signals	
1 - 8	2.2v with a front panel offset to allow ranges from –2.2v to 0v up to 0v to +2.2v, (shipped ±1.1v), 10 Mohm impedance, jumper block for 50 ohms
	Optional Differential Input, jumper block for 100ohm across line no front panel offset
Control Signals	
Clock In	TTL, 1k ohms to ground, 40Mhz to 80Mhz digitizer clock Positive going edge is the active edge The clock input must meet or exceed a minimum pulse width both high and low of 6.25ns
Trig In	TTL, 1k ohms to ground, Positive going edge is the active edge. Take number of samples set in Gate Duration Registers (0x20) & (0x22). Setting the Ext Gate Enabled bit in the Control Register (0x04) changes the function of the Trig/Gate input to the gate function. The gate input uses the positive going edge to start the digitizer and the negative going edge to stop instead of the settings in the Gate Duration Registers.
Indicator Leds	
Address	VME Access in progress
Active	Samples are being stored in memory.

CONNECTORS

The standard analog signal inputs are single ended and use single pin Lemo connectors, ERA.00.250,
2pin Lemo connectors are used for the optional differential inputs ERA.0S.302.
The Trig/Gate in and Clock in use standard single pin Lemo connectors, ERA.00.250

VME Addressing

The following **AM Codes** are used:

AM 2D or 29	Short Address A16	D16	Control & Status
AM 3D or 39	Standard Address A24 (if enabled)	D16	Broadcast Write Control only
AM 09 or 0D	Extended Address A32	D16/D32	Data Memory Read
AM 0B or 0F	A32 Block Transfer BLT32	D32 only	Data Memory Read
AM 08 or 0C	A32 64-Bit Block Transfer MBLT64	D64 only	Data Memory Read

The board occupies 256 bytes of Short (A16) and Standard (A24) Address space and 16 Mbytes of Extended Address (A32) space. for all memory options. The A16 Base Address is set with 2 hexadecimal switches selecting A8 - A15. The A32 Base Address (A24 to A31) is software settable in a register at A16 (0x1C). A24 is used for Broadcast Commands only (see 0x2E)

EXTENDED ADDRESS (A32) MEMORY MAP

The module must be disarmed to read the memory

DATA MEMORY SPACE

Channel	Up to 1M samples/channel Address A23 - A0
CH1	00 0000 - 3F FFFF
CH2	40 0000 - 7F FFFF
CH3	80 0000 - BF FFFF
CH4	C0 0000 - FF FFFF
CH5	00 0000 - 3F FFFF
CH6	40 0000 - 7F FFFF
CH7	80 0000 - BF FFFF
CH8	C0 0000 - FF FFFF

Note:

Channel addresses are interleaved
All addresses are +extended base address

See table below for Data Line Usage

Extended Block Transfer BLT32 cycles to 256 byte boundaries only (A0-7 = 0)
64-bit Block Transfer MBLT64 cycles to 2048 byte boundaries only (A0-10 = 0)

Category in 4-Byte group	**Data line usage**	**Category in 8-Byte group**	**Address and Data line usage**	**Byte Address**	**Chan / Sample #**
D32-BLT (BLT32)		**D64-MBLT** (MBLT64)			
Byte(0)	D[31..24]	Byte(0)	A[31..24]	xxxx…xxx000	
Byte(1)	D[23..16]	Byte(1)	A[23..16]	xxxx…xxx001	lsb Ch 5 / #1
Byte(2)	D[15..8]	Byte(2)	A[15..8]	xxxx…xxx010	
Byte(3)	D[7..0]	Byte(3)	A[7..1],Lword	xxxx…xxx011	lsb Ch 1 / #1
Byte(0)	D[31..24]	Byte(4)	D[31..24]	xxxx…xxx100	
Byte(1)	D[23..16]	Byte(5)	D[23..16]	xxxx…xxx101	lsb Ch 5 / #2
Byte(2)	D[15..8]	Byte(6)	D[15..8]	xxxx…xxx110	
Byte(3)	D[7..0]	Byte(7)	D[7..0]	xxxx…xxx111	lsb Ch 1 / #2

BROADCAST COMMAND ADDRESSING (A24)

The same command can be issued to multiple VTR8014 modules by enabling A24 Broadcast mode.
The A24 address and setup are stored at address 0x2E. VTR8014 modules with the same A24 address will accept the commands to that address. One VTR8014 is setup as the master and all the others with the same A24 address are setup as slaves. Only write cycles are accepted. Many different groups of modules may be created using different A24 addresses. This is particularly useful to arm, trigger or disarm modules as a group.

DATA READOUT:

The 14 bit digitized data for channels 1, 2, 3, and 4 is read out on D0-D13(MSB). The 14 bit digitized data for channels 5, 6, 7, and 8 is read out on D16-D29(MSB). An Over range bit can be jumper selected onto D14and D30. Ch1-4 jumper labeled 'D14", Ch5-8 jumper labeled 'D30'. Unused data bits D15 and D31 return logic zero. The output coding is straight binary.
The data is normally read out of the onboard memory after a digitizing cycle is complete, but another readout method is available similar to a free running ADC with readout 'on the fly'. See Read Last section above. See the Memory map for the data location of the channels.
The Memory Location Counter contains the next location to be filled with data. After a cycle, this is used to organize the data for readout. This is a word location and the value must be quadrupled for the bus memory address.

AVERAGING:

The VTR8014 can be setup to do averaging to raw ADC data before samples are stored in memory. The Averaging Setup Register (Base +8E) allows 7 settings for averaging or none. Sequential ADC samples are added, the total is divided by the number of samples added and the result is stored in memory. This increases the overall SNR of the module and also has the effect of giving an apparent slower sample rate. When in any averaging mode the Overflow bit is set if any ADC raw sample exceeds the comparator level

SHORT ADDRESS (A16) MEMORY MAP

Offset	Type		Function	
00	---	W	Master Reset Write only (no data looked at)	
02	D16	R	Status Register (see tables that follow for specs)	
04	D16	R/W	Control Register (see tables that follow for specs)	
06	D16	R/W	Interrupter Status/ID Register	
08	D16	R/W	Interrupter Set Up Register	
0A	D16	R/W	Clock Setup Register (Sampling Rate)	
0C	D16	R	ID Register, Module Type, Options and Serial Number	
0E	D16	R/W	Multiple Pre/Post Setup Register	
10	---	W	Internal (Software) Trigger	
12	---	W	Arm	
14	---	W	Disarm (Stop)	
16	---	W	Reset IRQ Source	
18	D16	W	Reset Memory Location Counter	
1A				
1C	D16	R/W	A32 Base Address Register, A31-A24 (A16 access only)	
1E	D16	R/W	Real Time Counter Setup Register	
20	D16	R/W	High Byte Gate Duration Register	The number of conversions following a trigger.
22	D16	R/W	Low Byte Gate Duration Register	
24	D16	R/W	High Byte Memory Location Counter	Word location. For Vme address the value must be quadrupled
26	D16	R/W	Low Byte Memory Location Counter	
28	D16	R/W	Event Register (# of post trigger events for Disarm and/or interrupt)	
2A	D16	R/W	Minimum PreTrigger Sample Register (# of PreTrigger samples before a Trigger is accepted)	
2C	D16	R/W	Trigger Delay Register	
2E	D16	R/W	Broadcast Command Setup Register (A24 Base Address and Enable)	
30	D16	R	Completed Post Trigger Cycles Counter Register (stored at Disarm)	
32	D16	R/W	Completed Post Trigger Cycles Counter (Write resets counter)	
34	D16	R/W	Last Address for each complete Post Trigger Cycle High byte first (read up to 510 times for 255 Addresses) Write will initialize readout to 1st stored address	
36	D16	R	Trigger Counter Register (stored at Disarm)	
38	D16	R	Trigger Counter (only valid if RTC is enabled)	
3A	D16	R/W	Real Time Counter Value for each Trigger (from memory High byte first (read up to 510 times for 255 Triggers) Write will initialize readout to 1st stored value	
3C	D16	R	High Byte Real Time Counter	direct readout of counter 'on the fly' not protected from readout errors
3E	D16	R	Low Byte Real Time Counter	
80	D16	R/W	Comparator Threshold Register CH1	
82 *	D16	W	Comparator Threshold Register ALL Channels	
84 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)	
86	D16	R	Last Conversion Data Register CH1	
8E	D16	R/W	Averaging Setup Register	

90	D16	R/W	Comparator Threshold Register CH2
92 *	D16	W	Comparator Threshold Register ALL Channels
94 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
96	D16	R	Last Conversion Data Register CH2
A0	D16	R/W	Comparator Threshold Register CH3
A2 *	D16	W	Comparator Threshold Register ALL Channels
A4 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
A6	D16	R	Last Conversion Data Register CH3
B0	D16	R/W	Comparator Threshold Register CH4
B2 *	D16	W	Comparator Threshold Register ALL Channels
B4 *	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
B6	D16	R	Last Conversion Data Register CH4
C0	D16	R/W	Comparator Threshold Register CH5
C2 *	D16	W	Comparator Threshold Register ALL Channels
C4 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
C6	D16	R	Last Conversion Data Register CH5
D0	D16	R/W	Comparator Threshold Register CH6
D2 *	D16	W	Comparator Threshold Register ALL Channels
D4 *	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
D6	D16	R	Last Conversion Data Register CH6
E0	D16	R/W	Comparator Threshold Register CH7
E2 *	D16	W	Comparator Threshold Register ALL Channels
E4 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
E6	D16	R	Last Conversion Data Register CH7
F0	D16	R/W	Comparator Threshold Register CH8
F2 *	D16	W	Comparator Threshold Register ALL Channels
F4 **	D16	R/W	Valid Data Register- all 8 Channels(see tables that follow)
F6	D16	R	Last Conversion Data Register CH8

Offset (A7-A0) from A16 (Short) Base address

NOTE: * = Any of these addresses can be used to write same data to ALL Channels simultaneously
**** = Any of these addresses can be used to read or reset ALL the Valid Data Bits**

MASTER RESET

Short Base + **00**H

Write only Data ignored, complete reset, same as SYSRESET or Power up
Resets all registers to zero and aborts any cycle.
Does not change channel memory data

STATUS REGISTER

Short Base + **02**H

D15-D8	NOT USED	
D7	1 = Averaging is Enabled (only valid if Digitizer is Armed)	READ ONLY
D6	1 = Post Trigger portion of cycle is in progress	READ ONLY
D5	1 = Digitizer is Triggered	READ ONLY
D4	1 = Memory Location Counter Overflow	READ ONLY
D3	1 = IRQ is Set (IRQ is on the Vmebus)	READ ONLY
D2	1 = IRQ Source is Set (Recording cycle is done, Active = 0)	READ ONLY
D1	1 = Digitizer is Active	READ ONLY
D0	1 = Digitizer is Armed	READ ONLY

CONTROL REGISTER

Short Base + **04**H

D15-D8	NOT USED	
D9	1 = Enable Minimum PreTrigger Samples to accept Trigger (see 0x2A)	R/W
D8	1 = Enable Disarm on Event Register Count (see 0x28)	R/W
D7	1 = Enable Delayed Trigger (see 0x2C)	R/W
D6	1 = Pre/Post Trigger Enabled	R/W
D5	1 = Ext Gate Enabled	R/W
D4	1 = Auto Reset Memory Location Counter with each Trigger	R/W
D3	1 = Wrap Mode Enabled	R/W
D2	1 = Disarm At End Of Cycle	R/W
D1*	1 = Enable Front Panel Trigger (defaults to Enabled)	R/W
D0*	1 = Enable Software Trigger (see add 10) (defaults to Enabled)	R/W

INTERRUPTER STATUS/ID REGISTER

Short Base + **06**H

D7	IRQ ID Bit 7, Returned during VME IACK Cycle	R/W
D6	IRQ ID Bit 6, Returned during VME IACK Cycle	R/W
D5	IRQ ID Bit 5, Returned during VME IACK Cycle	R/W
D4	IRQ ID Bit 4, Returned during VME IACK Cycle	R/W
D3	IRQ ID Bit 3, Returned during VME IACK Cycle	R/W
D2	IRQ ID Bit 2, Returned during VME IACK Cycle	R/W
D1	IRQ ID Bit 1, Returned during VME IACK Cycle	R/W
D0	IRQ ID Bit 0, Returned during VME IACK Cycle	R/W

INTERRUPTER SETUP REGISTER

Short Base + **08**H

D15-D8	NOT USED		
D7	NOT USED		
D6	NOT USED		
D4-5	0 = IRQ set on each Post Trigger Sample event completed (in post or pre/post modes) or end of FP Gate 1 = IRQ set on Disarm (from any source that disarms module) * 2 = IRQ set on Event Register = Completed Post Trigger Counter		R/W
D3 #	Interrupter IRQ ENABLE (1 = enabled)		R/W
D2 #	Interrupter Level Bit 2	Coded see below	R/W
D1 #	Interrupter Level Bit 1		R/W
D0 #	Interrupter Level Bit 0		R/W

* Module is Disarmed by:

- Master Reset
- Bus write to Short Base + 14H
- Completion of Post Trigger event (either Internal Gate Duration Register or Front Panel Gate) with 'Disarm at End of Cycle' = 1
- Completion of number of Post Trigger Events set in 0x28 if Enabled in Control Register
- End of single Pre/Post Cycle
- End of Selected number of Multi Pre/Post Cycles
- At Memory Counter Overflow if Wrap = 0

NOTE: Disable of IRQ also resets IRQ source

D0-D2	IRQ Level
0	No IRQ on Vmebus
1	1
2	2
3	3
4	4
5	5
6	6
7	7

CLOCK SETUP REGISTER (Sampling Clock)

Short Base + **0A**H

D15-D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	1 = External Clock Source	R/W
D2	Programmable Clock Frequency Select Bit 2	R/W
D1	Programmable Clock Frequency Select Bit 1	R/W
D0	Programmable Clock Frequency Select Bit 0	R/W

NOTE: No connection should be made to Front Panel Clock Input if using Internal Clock

BIT 0-2	Internal Clock Rate	External Clock Rate
0	80MHz (DEFAULT)	EXT CLK ÷ 1
1	40MHz	EXT CLK ÷ 2
2-7	not used	

MODULE ID REGISTER

Short Base + **0C**H

D15	Module Type &Options Bit 5	READ ONLY
D14	Module Type &Options Bit 4	READ ONLY
D13	Module Type &Options Bit 3	READ ONLY
D12	Module Type &Options Bit 2	READ ONLY
D11	Module Type &Options Bit 1	READ ONLY
D10	Module Type &Options Bit 0	READ ONLY
D9	Serial Number Bit 9	READ ONLY
D8	Serial Number Bit 8	READ ONLY
D7	Serial Number Bit 7	READ ONLY
D6	Serial Number Bit 6	READ ONLY
D5	Serial Number Bit 5	READ ONLY
D4	Serial Number Bit 4	READ ONLY
D3	Serial Number Bit 3	READ ONLY
D2	Serial Number Bit 2	READ ONLY
D1	Serial Number Bit 1	READ ONLY
D0	Serial Number Bit 0	READ ONLY

BIT 10-15	Module Type & Options
0	not used
1	VTR1012A
2	VTR3012A
3	VTR10010
4	VWG
5	VTR812
6	VTR812/40
7	VTR10012
8	VTR10012-8
9	VTR8014
10 - 15	not used
16	VS64 (TTL)
17	VS32 (TTL)
18	VS16 (TTL)
19	VS32 (ECL)
20	VS16 (ECL)
21	VS32 (NIM)
22	VS16 (NIM)
23	VS64D (TTL)
24	VS32D (TTL)
25	VS16D (TTL)
26	VS32D (ECL)
27	VS16D (ECL)
28	VS32D (NIM)
29	VS16D (NIM)
30 - 63	not used

MULTI PRE/POST SETUP REGISTER

Short Base + **0E**H

D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	NOT USED	
D3	NOT USED	
D2	1 = ENABLE MULTI PRE/POST MODE	R/W
D1	NUMBER OF SEGMENTS BIT 2	R/W
D0	NUMBER OF SEGMENTS BIT 1	R/W

SEGMENT CODING

BIT 0-1	Total Memory Divided Into
0	2 Segments
1	4 Segments
2	8 Segments
3	16 Segments

INTERNAL (SOFTWARE) TRIGGER

Short Base + 10H

Write only, Data ignored. Must be Enabled
Same as front panel Trig input
Can be a Broadcast Command (see 0x2E)

ARM

Short Base + 12H

Write only, Data ignored. Sets Digitizer Armed bit
Also sets Active if Pre/Post or Multi Pre/Post is enabled
Can be a Broadcast Command (see 0x2E)

DISARM

Short Base + 14H

Write only, Data ignored. Clears Armed bit and Stops Digitizer
To abort a PrePost cycle, clear the setup bits for PrePost also (0x04 bit D6 or 0x0E bit D2)
Can be a Broadcast Command (see 0x2E)

CLEAR IRQ SOURCE & REQUEST

Short Base + 16H

Write only, Data ignored. Clears IRQ Source and removes request from Vmebus.
Can be a Broadcast Command (see 0x2E)

RESET MEMORY LOCATION COUNTER

Short Base + **18**H

Write only, Data ignored. Resets Memory Location and Post Trigger Counter to zero.
Can be a Broadcast Command (see 0x2E)

A32 BASE ADDRESS REGISTER

Short Base + **1C**H

D7	1 = A31 Added for A32 Base Address	R/W
D6	1 = A30 Added for A32 Base Address	R/W
D5	1 = A29 Added for A32 Base Address	R/W
D4	1 = A28 Added for A32 Base Address	R/W
D3	1 = A27 Added for A32 Base Address	R/W
D2	1 = A26 Added for A32 Base Address	R/W
D1	1 = A25 Added for A32 Base Address	R/W
D0	1 = A24 Added for A32 Base Address	R/W

REAL TIME COUNTER SETUP REGISTER

Short Base + **1E**H

D15-D2	NOT USED	
D1	RTC Select Bit 1	R/W
D0	RTC Select Bit 0	R/W

NOTE: RTC starts with ARM

BIT 0-1	Clock Rate	Period
0	OFF (DEFAULT)	
1	80MHz	12.5ns
2	40MHz	25ns
3	8MHz	125ns

GATE DURATION REGISTERS (# of Post Trigger samples)

HIGH BYTE

Short Base + 20H

D15-D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	1= 1048576 Samples	R/W
D3	1= 524288 Samples	R/W
D2	1= 262144 Samples	R/W
D1	1= 131072 Samples	R/W
D0	1= 65536 Samples	R/W

LOW BYTE

Short Base + 22H

D15	1= 32768 Samples	R/W
D14	1= 16384 Samples	R/W
D13	1= 8192 Samples	R/W
D12	1= 4096 Samples	R/W
D11	1= 2048 Samples	R/W
D10	1= 1024 Samples	R/W
D9	1= 512 Samples	R/W
D8	1= 256 Samples	R/W
D7	1= 128 Samples	R/W
D6	1= 64 Samples	R/W
D5	1= 32 Samples	R/W
D4	1= 16 Samples	R/W
D3	1= 8 Samples	R/W
D2	1= 4 Samples	R/W
D1	1= 2 Samples	R/W
D0	1= 1 Sample	R/W

Note: Recommended minimum Gate Duration of 4 samples.
To calculate Gate Duration (# of post trigger samples) add samples of selected bits.

MEMORY LOCATION COUNTER

HIGH BYTE

Short Base + 24H

D15-D8	NOT USED	
D7	NOT USED	
D6	NOT USED	
D5	NOT USED	
D4	1= 1048576	Read Only
D3	1= 524288	Read Only
D2	1= 262144	Read Only
D1	1= 131072	Read Only
D0	1= 65536	Read Only

LOW BYTE

Short Base + 26H

D15	1= 32768	Read Only
D14	1= 16384	Read Only
D13	1= 8192	Read Only
D12	1= 4096	Read Only
D11	1= 2048	Read Only
D10	1= 1024	Read Only
D9	1= 512	Read Only
D8	1= 256	Read Only
D7	1= 128	Read Only
D6	1= 64	Read Only
D5	1= 32	Read Only
D4	1= 16	Read Only
D3	1= 8	Read Only
D2	1= 4	Read Only
D1	1= 2	Read Only
D0	1= 1	Read Only

NOTE: Add values for Lword Location, for memory address the value must be quadrupled.

EVENT REGISTER (65535 max)

Short Base + 28H

16 bit register which contains the number of Completed Post Trigger Cycles to run before setting an Interrupt and /or Disarming. See Interrupter Setup Register (0x08) and Control Register (0x04) to enable this feature Cleared by Master Reset

Minimum PreTrigger Sample Register (65535 max)

Short Base + 2AH

16 bit register which contains the number of PreTrigger samples to be recorded after Arm before a Trigger is accepted. See the Control Register (0x04) to enable this feature

Cleared by Master Reset

:

TRIGGER DELAY SETUP REGISTER

Short Base + 2CH

D15	1= 32768 Samples	R/W
D14	1= 16384 Samples	R/W
D13	1= 8192 Samples	R/W
D12	1= 4096 Samples	R/W
D11	1= 2048 Samples	R/W
D10	1= 1024 Samples	R/W
D9	1= 512 Samples	R/W
D8	1= 256 Samples	R/W
D7	1= 128 Samples	R/W
D6	1= 64 Samples	R/W
D5	1= 32 Samples	R/W
D4	1= 16 Samples	R/W
D3	1= 8 Samples	R/W
D2	1= 4 Samples	R/W
D1	1= 2 Samples	R/W
D0	1= 1 Sample	R/W

Note: Recommended minimum Trigger Delay of 2 samples.

To calculate Trigger Delay add samples of selected bits Multiply by the period of the selected sample clock for the Time value.

BROADCAST COMMAND SETUP REGISTER

(set A24 base address and Enable Broadcast participation)

Short Base + **2EH**

D9	1 = Enable Broadcast Participation	R/W
D8	1 = Master (0 = Slave)	R/W
D7	1 = A23 Added for A24 Base Address	R/W
D6	1 = A22 Added for A24 Base Address	R/W
D5	1 = A21 Added for A24 Base Address	R/W
D4	1 = A20 Added for A24 Base Address	R/W
D3	1 = A19 Added for A24 Base Address	R/W
D2	1 = A18 Added for A24 Base Address	R/W
D1	1 = A17 Added for A24 Base Address	R/W
D0	1 = A16 Added for A24 Base Address	R/W

COMPLETED POST TRIGGER CYCLES COUNTER REGISTER (65535 max)

Short Base + 30H

Read only, 16 bit Register that stores the value of the Completed Post Trigger Cycle Counter at Disarm, only reset by Master Reset. and valid until next Disarm.

COMPLETED POST TRIGGER CYCLES COUNTER (65535 max)

Short Base + 32H

16 bit counter which counts Completed Post Trigger Cycles, may be read while armed
reset by Master Reset, write to this address or any Memory Location Counter Reset

READ LAST ADDRESS FOR EACH COMPLETED POST TRIGGER CYCLE (255 max)

Short Base + 34H

Sequential readout of the 21bit Last Memory Location for each completed Post Trigger Cycle. High byte first, read up to 510 times for 255 triggers. Write to this address to reset the readout pointer to 1st location before reading (it is not necessary to read to end and rereading is also possible). Data is valid until next arm. Data is from a memory, which is not necessarily all overwritten so data is only valid for number in the Completed Post Trigger Cycles Counter Register.

The memory will be overwritten if more than 255 completed events are stored. Therefore the Event Register should be used to set an interrupt when this memory is full and disarm the module. Otherwise the *last* 255 events will be stored.

For VME memory address the value must be quadrupled.

TRIGGER COUNTER REGISTER (255 max)

Short Base + 36H

Read only, 8 bit Register that stores the value of the Trigger Counter at Disarm, RTC must be enabled. only reset by Master Reset. and valid until next Disarm.

TRIGGER COUNTER (255 max)

Short Base + 38H

8 bit counter which counts received Triggers, only valid while armed. RTC must be enabled
reset by Disarm and by Master Reset

REAL TIME COUNTER (RTC) VALUE FOR EACH TRIGGER (255 max)

Sequential readout of the 32bit Real Time Counter value when each trigger was received. RTC must be enabled (+3Eh).. The memory can only store 255 Trigger times and if more than 255 triggers are received the last 255 will be stored. To stop overwriting this memory, use the Events Register to set an interrupt when this memory is full and disarm the module. High byte first, read up to 510 times for 255 triggers. Write to this address to reset the readout pointer to 1st location before reading (it is not necessary to read to end and rereading is also possible). Data is valid until next arm. Data is from a memory which is not necessarily all overwritten so data is only valid for number in the Trigger Counter Register. Data is valid until next arm.

Read the Trigger Counter Register (+36h) for total valid times stored, Write to +38h to reset the readout pointer to the 1st location and then read this address (+3Ah) twice for each valid time. Data is returned High Word then Low Word for each time. Each bit has a value set by the period of the selected clock (+1E).

HIGH WORD (1st Read)

Short Base + **3A**H

D15	1= 2 147 483 648	Read Only
D14	1= 1 073 741 824	Read Only
D13	1= 536 870 912	Read Only
D12	1= 268 435 456	Read Only
D11	1= 134 217 728	Read Only
D10	1= 67 108 864	Read Only
D9	1= 33 554 432	Read Only
D8	1= 16 777 216	Read Only
D7	1= 8 388 608	Read Only
D6	1= 4 194 304	Read Only
D5	1= 2 097 152	Read Only
D4	1= 1 048 576	Read Only
D3	1= 524 288	Read Only
D2	1= 262 144	Read Only
D1	1= 131 072	Read Only
D0	1= 65 536	Read Only

LOW WORD (2nd Read)

Short Base + **3A**H

D15	1= 32768	Read Only
D14	1= 16384	Read Only
D13	1= 8192	Read Only
D12	1= 4096	Read Only
D11	1= 2048	Read Only
D10	1= 1024	Read Only
D9	1= 512	Read Only
D8	1= 256	Read Only
D7	1= 128	Read Only
D6	1= 64	Read Only
D5	1= 32	Read Only
D4	1= 16	Read Only
D3	1= 8	Read Only
D2	1= 4	Read Only
D1	1= 2	Read Only
D0	1= 1	Read Only

COMPARATOR THRESHOLD REGISTERS

Short Base + **80**H Channel 1
Short Base + **90**H Channel 2
Short Base + **A0**H Channel 3
Short Base + **B0**H Channel 4
Short Base + **C0**H Channel 5
Short Base + **D0**H Channel 6
Short Base + **E0**H Channel 7
Short Base + **F0**H Channel 8

D15	not used	
D14	not used	
D13	1= 8192	R/W
D12	1= 4096	R/W
D11	1= 2048	R/W
D10	1= 1024	R/W
D9	1= 512	R/W
D8	1= 256	R/W
D7	1= 128	R/W
D6	1= 64	R/W
D5	1= 32	R/W
D4	1= 16	R/W
D3	1= 8	R/W
D2	1= 4	R/W
D1	1= 2	R/W
D0	1= 1	R/W

NOTE: Value is in Straight Binary. Value is 0.134mv per bit

To write ALL registers simultaneously use ANY of these addresses: 82, 92 A2 ,B2 ,C2 ,D2 ,E2 or F2

VALID DATA REGISTER

Use ANY of the following addresses

Short Base + **84**H, **94**H, **A4**H, **B4**H, **C4**H, **D4**H, **E4**H, or **F4**H

READ Valid Data Register

D0	D1	D2	D3	D4	D5	D6	D7
CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8

Dx = 1 = At least 1 sample was greater than comparator threshold register value
Dx = 0 = No samples were greater than comparator threshold register value
D8 - D15 are not used and return '0'

WRITE Valid Data Register

A Write cycle (data ignored) to ANY of the following addresses clears ALL valid data bits

Short Base + **84**H, **94**H, **A4**H, **B4**H, **C4**H, **D4**H, **E4**H, or **F4**H

LAST CONVERSION DATA REGISTERS #

Short Base + **86**H Channel 1
Short Base + **96**H Channel 2
Short Base + **A6**H Channel 3
Short Base + **B6**H Channel 4
Short Base + **C6**H Channel 5
Short Base + **D6**H Channel 6
Short Base + **E6**H Channel 7
Short Base + **F6**H Channel 8

D15	not used- return 0	
D14	1 = Overflow if jumped on Bd	Read Only
D13	1= 8192	Read Only
D12	1= 4096	Read Only
D11	1= 2048	Read Only
D10	1= 1024	Read Only
D9	1= 512	Read Only
D8	1= 256	Read Only
D7	1= 128	Read Only
D6	1= 64	Read Only
D5	1= 32	Read Only
D4	1= 16	Read Only
D3	1= 8	Read Only
D2	1= 4	Read Only
D1	1= 2	Read Only
D0	1= 1	Read Only

NOTE: Value is in Straight Binary. Value is 0..134mv per bit

This 'on the fly' readout is available with digitizer armed or unarmed but it can contain large errors due to asynchronous operation of the read cycles verses the digitizer clock. Use for setup/test only.

AVERAGING SETUP REGISTER

Short Base + **8E**H

D15-D3	NOT USED	
D2	Averaging Select Bit 2	R/W
D1	Averaging Select Bit 1	R/W
D0	Averaging Select Bit 0	R/W

BIT 0-1	Samples to Average	Apparent ADC Sample Rate *
0	OFF (DEFAULT)	80MHz
1	2	40MHz
2	4	20MHz
3	8	10MHz
4	16	5MHz
5	32	2.5MHz
6	64	1.25MHz
7	128	0.625MHz

* NOTE: Based on 80 MHz Clock

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