

Howard Univ.



**Model 850
Quad Single-Channel Analyzer
Operating and Service Manual**

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Quad Single-Channel Analyzer
Operating and Service Manual

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for
EG&G ORTEC Instruments

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Damage in Transit

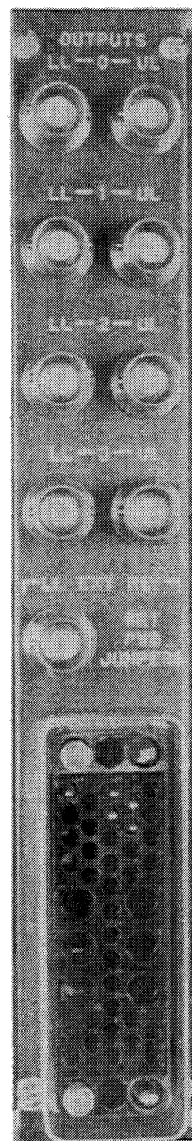
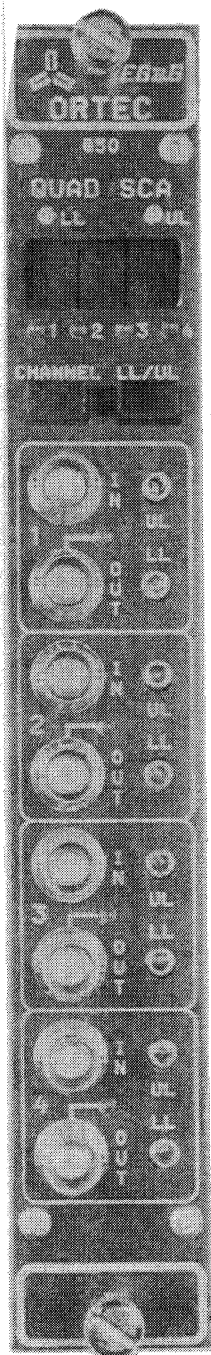
Shipments should be examined immediately upon receipt for evidence of external or concealed damage. The carrier making delivery should be notified immediately of any such damage, since the carrier is normally liable for damage in shipment. Packing materials, waybills, and other such documentation should be preserved in order to establish claims. After such notification to the carrier, please notify EG&G ORTEC of the circumstances so that assistance can be provided in making damage claims and in providing replacement equipment, if necessary.

CONTENTS

	Page
WARRANTY	ii
PHOTOGRAPHS	iv
1. DESCRIPTION	1
1.1. General	1
1.2. Modes of Operation	1
1.3. Leading Edge Timing	1
1.4. Lower-Level Reference	1
2. SPECIFICATIONS	2
2.1. Performance	2
2.2. Controls	2
2.3. Inputs	2
2.4. Outputs	2
2.5. Related Equipment	2
2.6. Electrical and Mechanical	2
3. INSTALLATION	3
3.1. Connection to Power	3
3.2. Connection from Linear Amplifier	3
3.3. Output Connections	3
3.4. Lower-Level Reference Input	3
4. OPERATING INSTRUCTIONS	4
5. CIRCUIT DESCRIPTION	5
5.1. General	5
5.2. Block Diagram	5
5.3. Detailed Circuit Description	5
6. MAINTENANCE AND CALIBRATION	7
6.1. General	7
6.2. Factory Repair	7
6.3. Tabulated Test Point Voltages	7
COMPONENT DRAWINGS AND SCHEMATICS	

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EG&G ORTEC MODEL 850 QUAD SINGLE-CHANNEL ANALYZER

1. DESCRIPTION

1.1. GENERAL

The EG&G ORTEC 850 Quad Single-Channel Analyzer has the exceptionally wide dynamic range, the stability, and the high resolution necessary for use in high-resolution HPGe spectroscopy experiments. These same features provide more than adequate performance with scintillation counters and ionization chambers. Dc-coupled input, integrated circuit discriminators, and logic are employed to obtain these characteristics and to assure maximum performance at high counting rates.

The 850 accepts either positive unipolar or bipolar input pulses from linear amplifiers that have either active, RC, or delay-line shaping. The amplitude of each input pulse is examined, and appropriate NIM-standard positive logic output pulses are generated separately for SCA, LLD, and ULD responses. The instrument is designed to meet the recommended interchangeability standards of USAEC Report TID-20893 (Rev). An EG&G ORTEC 4001A/402D Bin and Power Supply provides all the necessary power (including +6 V) through the rear module power connector. All signal levels and impedances are compatible with other EG&G ORTEC modules.

1.2. MODES OF OPERATION

The 850 consists of four completely independent channels of single-channel analyzer. Each channel has a set of four printed wiring board (PWB) jumpers (accessible through the side panel) that control the operation of the unit. The function of each jumper is labeled on the side panel. Channel SCA1 jumpers are labeled W1 through W4. Jumper W1 selects dc- or ac-coupled input. Jumper W2 selects the front-panel LL potentiometer or the voltage signal applied to the rear-panel LL Ref Ext connector as the LL discriminator reference threshold. Jumpers W3 and W4 select the mode of operation as either Integral, Normal, or Window.

The 850 has an easy-to-use, built-in digital voltmeter for setting the Lower-Level and Upper-Level thresholds of each channel. A front-panel push button selects which of the four channels is being read. A second front-panel push button selects either the Lower-Level or the Upper-Level reading. Each threshold can be set over the range from 20 mV to 9.99 V. In the Window mode, the range of setting is 2 mV to 0.999 V. The digital voltmeter reading must be divided by 10 to determine the Window setting. The display flashes on overrange.

INTEGRAL MODE In the Integral mode, each channel of the 850 provides an output signal to the Out connector on the front panel if the input pulse amplitude exceeds the adjusted Lower-Level threshold. The input range is 0 to 10 V. For Integral mode operation, jumper W3 must be in the Intg/Norm position, and jumper W4 must be in the Intg position.

NORMAL MODE In the Normal mode, the 850 provides an output pulse to the Out connector on the front panel if the input pulse amplitude exceeds the Lower-Level threshold but does not exceed the Upper-Level threshold. In this mode, each threshold is adjusted independently in the range of 20 mV to 9.99 V, and the ULD level must be set higher than the LLD level to permit the SCA output to be generated. For Normal mode operation, jumper W3 must be in the Intg/Norm position, and jumper W4 must be in the Norm/Win position.

WINDOW MODE In the Window mode, the 850 provides an output pulse to the Out connector on the front panel if the input pulse amplitude exceeds the Lower-Level threshold, but by an amount that is less than the adjusted window width. The range of the LLD is 20 mV to 9.99 V, and the range of the window is adjusted from 2 mV to 0.999 V above the LLD level. This mode is especially adapted to high-resolution spectroscopy because the very narrow windows that are required for this type of operation are reproducible and easy to obtain. For Window mode operation, jumper W3 must be in the Win position, and jumper W4 must be in the Norm/Win position.

The SCA output pulses from each channel of the 850 are generated when the trailing edge of the input signal being analyzed crosses the Lower-Level threshold, provided the LLD and ULD threshold requirements have been met. For this reason, the 850 cannot be used effectively for crossover timing applications.

1.3. LEADING EDGE TIMING

Connectors are included on the rear panel for LL and UL outputs for each channel of the 850. The pulses that are furnished through these connectors are generated on the leading edge of the input signal, each one occurring when the corresponding discriminator is triggered by the input pulse amplitude. Either of these pulses can be used for timing applications or for pulse-routing into a multichannel analyzer. In any mode of operation, either the LL or the UL output can be used to monitor the number of input pulses that cross the corresponding threshold.

1.4. LOWER-LEVEL REFERENCE

Each channel of the 850 has a PWB jumper, W2, that selects either the front-panel Lower-Level control or the voltage signal applied through the rear-panel LL Ext Ref connector as the reference level for the Lower-Level discriminator. This permits flexibility in operation when an external reference source can furnish the LLD with a stepped- or sliding-threshold to automatically sweep the SCA response through a spectral range.

2. SPECIFICATIONS

2.1. PERFORMANCE

DYNAMIC RANGE 500:1.

PULSE-PAIR RESOLVING TIME 200 ns plus output pulse width.

THRESHOLD TEMPERATURE INSTABILITY $\leq \pm 0.01\%$ / °C of full scale, 0 to 50°C using a NIM class-A power supply (referenced to -12 V).

WINDOW WIDTH INCONSISTENCY $< \pm 0.1\%$ variation of full-scale window width over the linear 0- to 10-V input range.

DISCRIMINATOR NONLINEARITY $< \pm 0.25\%$ of full scale (integral) for both discriminators.

2.2. CONTROLS

WINDOW OR UPPER LEVEL Front-panel screwdriver potentiometer determines the window width (0 to 1 V) in the Window mode or the Upper-Level (20 mV to 9.99 V) threshold in the Normal mode. This control is disabled in the Integral mode. The built-in voltmeter is used to read the Window- or Upper-Level setting.

LOWER LEVEL Front-panel screwdriver potentiometer (adjustable from 20 mV to 9.99 V) determines the threshold setting for the Lower-Level discriminator when the PWB LL Ref mode jumper is set on Int. When the LL Ref mode jumper is in the Ext position, the control is ineffective.

INTEGRAL/NORMAL/WINDOW Two PWB jumpers select one of three operating modes:

Integral LL sets a single discriminator threshold (20 mV to 9.99 V) and UL is disabled.

Normal UL and LL are independently adjustable levels (20 mV to 9.99 V).

Window LL sets the baseline level (20 mV to 9.99 V) and UL sets the window width (2 mV to 0.999 V). The Digital Voltmeter reading must be divided by 10 to determine the Window setting.

LL REF MODE A PWB jumper selects either the front-panel LL potentiometer or the voltage signal applied to the rear-panel LL Ref Ext connector as the LL discriminator reference threshold.

DIGITAL VOLTMETER

Channel Front-panel push button to select channel 1 through 4. Front-panel red LED indicates the selected channel.

LL/UL Front-panel push button selects Lower-Level or Upper-Level threshold for viewing on the Digital Volt-

meter. Front-panel yellow LED indicates the selected threshold.

Inaccuracy ± 1 digit.

2.3. INPUTS

SIGNAL INPUTS Front-panel BNC connector accepts positive, unipolar or bipolar signal, 0- to 10-V linear range. PWB jumper selects either dc- or ac-coupled input. For dc-coupled input, ± 12 V maximum; width > 100 ns; $Z_{in} = 1$ k Ω . For ac-coupled input, ± 100 V maximum; 0.2- to 10- μ s width; $Z_{in} = 1$ k Ω .

LL REF EXT When the PWB jumper is on Ext, the rear-panel BNC connector accepts the Lower-Level biasing. (An input of -20 mV to -9.99 V on this connector corresponds to a range of 20 mV to 9.99 V for the Lower-Level discriminator setting.) Input protected to ± 24 V.

2.4. OUTPUTS.

SCA OUT Front-panel BNC connector provides positive NIM-standard output, nominally +5 V; 500 ns wide; $Z_o \leq 10$ Ω . Output occurs as the trailing edge of linear input crosses the LL threshold.

LL OUT Rear-panel BNC connector provides positive NIM-standard output, nominally +5 V; 500 ns wide; $Z_o \leq 10$ Ω . Output occurs as the leading edge of linear input crosses the LL threshold.

UL OUT Rear-panel BNC connector provides positive NIM-standard output, nominally +5 V; 500 ns wide; $Z_o \leq 10$ Ω . Output occurs as leading edge of linear input crosses the UL threshold.

2.5. RELATED EQUIPMENT

The 850 is compatible with all EG&G ORTEC amplifiers and other amplifiers having a 0- to 10-V positive, linear output range.

2.6. ELECTRICAL AND MECHANICAL

POWER REQUIRED +12 V, 145 mA; -12 V, 140 mA; +6 V, 400 mA.

WEIGHT

Net 0.91 kg (2.0 lb).

Shipping 2.27 kg (5.0 lb).

DIMENSIONS NIM-standard single-width module, 3.43 x 22.13 cm (1.35 x 8.714 in.) per TID-20893 (Rev).

3. INSTALLATION

Since the 850 contains no internal power supply, it is used in conjunction with an EG&G ORTEC 4001A/402D NIM Bin and Power Supply, which is intended for rack mounting. Note that the power supply must provide +6 V as well as ± 12 V and ± 24 V. If vacuum tube equipment or any other source of heat is operated in the same rack, there must be sufficient cooling air circulating to prevent any localized heating of the transistorized circuitry used throughout the 850. The temperature of equipment mounted in racks can easily exceed the recommended maximum unless precautions are taken; the 850 should not be subjected to temperatures in excess of 120°F (50°C).

3.1. CONNECTION TO POWER

Turn off the bin power supply when inserting or removing modules. Power supply voltages should be checked after the modules have been inserted. Use the test points on the power supply control panel of the EG&G ORTEC 4001A/402D Bin and Power Supply to monitor dc voltages.

When operating the 850 outside the 4001A/402D Bin and Power Supply, be sure that the power extension cable that is used properly accounts for the power supply grounding circuits that are provided according to the recommended AEC standards outlined in TID-20893 (Rev). Both high-quality and power-return ground connections are provided to ensure proper reference voltage feedback into the power supply, and these must be preserved in remote cable installations. Take care to avoid ground loops when the module is operated outside the bin.

3.2. CONNECTION FROM LINEAR AMPLIFIER

Each channel of the 850 has a front-panel input to be used for the analog signals that are furnished from a linear amplifier. The front-panel BNC can be set as a dc-coupled path or as an ac-coupled path using the W1 connector accessible through the side panel. The dc-coupled path is generally preferred. However, if there is an dc-baseline offset, if signal amplitudes exceed the +12 V maximum limit or the dc circuit, or if the input pulses decay slowly, ac-coupling is available by proper setting of the W1 jumper.

Either input circuit accepts positive unipolar pulses or bipolar pulses (the positive lobe will be analyzed) into an input impedance of 1 k Ω . When cables more than 1.5-meters long are used to connect the amplifier output to the 850 input, cable termination may be necessary in order to prevent reflections. In this case, the cable impedance must be matched with a terminator at the 850 input.

The input operating range is from the Lower-Level threshold, typically <20 mV minimum to 10 V. This range is compatible with the range of output pulses that are normally available from NIM-modular linear amplifiers and biased amplifiers.

3.3. OUTPUT CONNECTIONS

A logic output pulse is available at the front-panel BNC connector when input pulses satisfy the amplitude and logic requirements of the 850. When the 850 is set for either differential single-channel mode (normal or window), the logic output pulse indicates that the input pulse amplitude is sufficient to trigger the Lower-Level discriminator without also triggering the Upper-Level discriminator. When the 850 is set for Integral mode of operation, the logic output indicates that the input pulse amplitude is sufficient to trigger the Lower-Level discriminator.

Separate logic outputs are available through the rear panel to indicate when, on the leading edge of an input pulse, each of the two discriminators is triggered. These responses can be used to monitor the discriminator levels during adjustment, to be counted in external counters, or to provide subgroup routing in a multichannel analyzer.

Each logic output is a NIM-standard slow positive pulse that is compatible with all EG&G ORTEC counters, counting rate meters, and other instruments. The output impedance of each output is sufficiently low to drive as many as ten paralleled 1-k Ω inputs.

3.4. LOWER-LEVEL REFERENCE INPUT

Each channel of the 850 has a PWB jumper to allow selection of an external reference level for the Lower-Level discriminator. When the LL Ref jumper, W2, is set in the Ext position, the front-panel Lower-Level control is disconnected, and the reference level must be furnished through the LL Ext Ref connector on the rear panel. An input of 0 to -10 V through this connector corresponds directly to a range of 0 to +10 V for the Lower-Level discriminator threshold.

If an input is connected to the LL Ref connector, only those channels with W2 set in the Ext position will have the LL reference derived from the LL Ext Ref signal. All channels with W2 set in the Int position will have the Lower-Level reference derived from the front-panel control.

The front-panel voltmeter will read the Lower-Level value when jumper W2 is set in either the Int or the Ext position.

4. OPERATING INSTRUCTIONS

Prior to operation, each channel of the 850 should be set in the desired configuration. Four PWB jumpers are available in each channel to select Integral, Normal, or Window mode; Internal or External Lower-Level reference; and dc- or ac-coupled input. Once the 850 is properly configured, it can be connected into a system according to the installation information in Section 3.

Figure 4.1 illustrates the timing relationships that will be effective in the 850 for each of two possible input pulse conditions. One is a pulse that exceeds the Lower-Level threshold without also exceeding the Upper-Level, and the other is a pulse that exceeds both thresholds. If the 850 is configured in the Integral mode, there is an SCA output pulse for each of the input pulses generated when the trailing edge of the input pulse crosses through the LLD level. If the 850 is configured in either the Normal or Window mode and operates in a differential single-channel analyzer mode, an SCA output pulse is generated for the first pulse but not for the second. For either mode,

the LL Out and the UL Out signals are available when the corresponding discriminator is triggered on the leading edge of the input pulse.

The adjusted Lower-Level threshold is furnished either by the front-panel Lower-Level control or from a dc-bias level through the rear-panel LL Ref connector; the alternate selection is made with the W2 PWB jumper. In either case, the range is from 20 mV to 9.99 V, measured on the analog input pulse. The value of the Lower-Level threshold can be read using the built-in front-panel voltmeter.

The adjusted Upper-Level threshold is determined by the setting of the front-panel Upper-Level control. When the 850 is configured in the Window mode, the range of the control is from 2 mV to 0.999 V. The front-panel voltmeter reading must be divided by 10 to obtain the proper value of the Window setting. When the 850 is configured in the Normal mode, the range of the control is from 20 mV to 9.99 V. The value of the Upper-Level threshold can be read directly by using the built-in front-panel voltmeter.

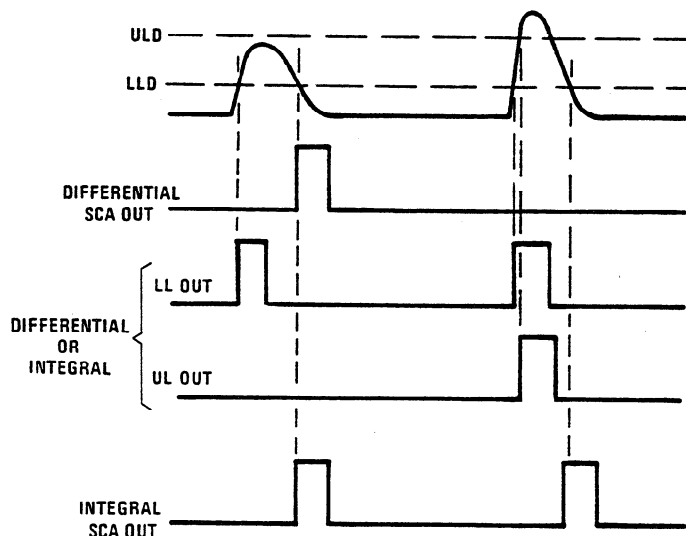


Fig. 4.1. Timing Relationships for Input and Output Pulses.

5. CIRCUIT DESCRIPTION

5.1. GENERAL

The EG&G ORTEC 850 Quad Single-Channel Analyzer has the exceptionally wide dynamic range, the stability, and the high resolution necessary for use in high-resolution HPGe spectroscopy experiments. These same features provide more than adequate performance with scintillation counters and ionization chambers. Decoupled input, integrated circuit discriminators, and logic are employed to obtain these characteristics and to assure maximum performance at high counting rates.

The 850 consists of four completely independent channels of single-channel analyzer. Each channel is versatile, with three basic operating modes provided. In the Window mode, each channel operates as a high-resolution, narrow window (0 to 10%), single-channel analyzer. For wide window applications the Normal mode is used. In this mode the Upper-Level and Lower-Level controls of each channel are independently variable from 20 mV to 9.99 V, and an output is generated for pulses analyzed between the levels. A front-panel green LED indicates activity. Through the use of separate rear-panel LL Out and UL Out outputs, each channel can operate as a dual wide-dynamic range integral discriminator for leading-edge timing or for pulse routing.

For an application where it is desirable to investigate an entire spectrum, an external baseline sweep input is provided via the rear-panel LL Ref Ext BNC connector. PWB jumpers select which of the four channels will use the external baseline sweep. In this mode of operation the baseline (Lower-Level threshold) on which a window is riding is swept through an energy range and count rate is recorded as a function of energy.

The 850 has an easy-to-use built-in digital voltmeter for setting the Lower-Level and Upper-Level thresholds of each channel. A front-panel push button selects which of the four channels is being read. A second front-panel push button selects either the Lower-Level or the Upper-Level reading. The digital voltmeter display flashes on overrange.

5.2. BLOCK DIAGRAM

Figure 5.1 is a simplified block diagram of one section of the 850 Quad SCA. This figure illustrates that each input pulse is furnished to both a Lower-Level and an Upper-Level discriminator, and that each discriminator generates an output pulse if its respective threshold is exceeded by the input signal amplitude. The discriminator thresholds are set independently for the Integral or Normal mode selection. For Window operation, the threshold for the UL discriminator is based on the LL setting instead of ground.

If the mode jumpers, W3 and W4, are in the Integral position, each LL response generates an SCA output. With the mode jumpers set at either Normal or Window, an SCA output is generated if the LL discriminator is triggered and the UL discriminator is not triggered.

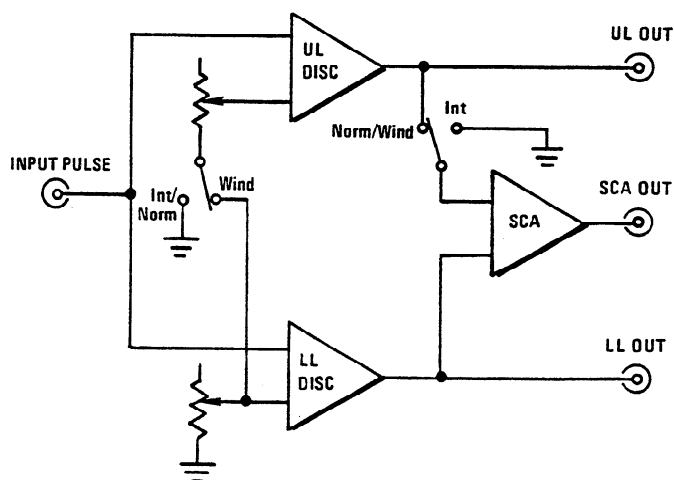


Fig. 5.1. Simplified Block Diagram of the 850 Quad SCA.

Timing is not indicated in Fig. 5.1. The LL Out and the UL Out signals are generated on the leading edge of the input analog signal. The SCA Out signal is generated on the trailing edge of the input signal, after the threshold criteria have been tested.

5.3. DETAILED CIRCUIT DESCRIPTION

A schematic diagram and component assembly drawing of the 850 are included at the back of this manual. Each of the four SCA sections are identical and only one detailed schematic is shown. Component designators for channel 1 have a "1" prefix; for channel 2 a "2" prefix; for channel 3 a "3" prefix; and for channel 4 a "4" prefix. Thus the component values of 1R1, 2R1, 3R1, and 4R1 are the same since they correspond to the same component in each of the four channels. Components in the voltmeter section do not have a prefix on their component designation. Several of the integrated circuits used in the 850 are multi-function. A unique subsection within an IC is indicated by the IC reference designator followed by the specific pin number in parentheses. For example, 1U1(1) indicates the output terminal of one op-amp of the quad op-amp in 1U1.

INPUT CIRCUIT Channel 1 is shown on page 1 of the 2-page schematic diagram. The analog input signal to channel 1 is divided by two by 1R29 and 1R25 before being fed to the LL comparator at 1U3(3) and the UL comparator at 1U2(3).

LOWER-LEVEL CIRCUIT The LL circuitry is built around a fast comparator, 1U3. The lower level is set by the front-panel potentiometer, 1R2, and is referenced to the -12-V NIM power supply. The setting on 1R2 is buffered by the unity gain stage 1U1(1) and the unity gain inverting stage 1U1(7) before being fed to the LL comparator at 1U3(4). The minimum value of the lower-level reference is set at 20 mV by 1R11. Offset voltages within

the lower-level circuitry are compensated by the factory-set PWB potentiometer 1R6.

When the positive-going analog input signal causes 1U3(3) to become more positive than the LL-reference level at 1U3(4), output 1U3(11) goes positive. This crossing of the lower level is latched in the set-reset flip-flop made up of the internal gate of 1U3 and gate 1U4(1). The second output at 1U3(9) connects to the input 1U3(4) through 1R28 to provide hysteresis to the lower-level comparator and prevent oscillations as the input signal crosses the lower-level reference voltage.

The positive-going signal at 1U3(11) triggers a negative-going one-shot signal at 1U7(4). This signal, nominally 500 ns wide, drives the hybrid output driver 1A2 which furnishes the LL Out signal on the rear panel.

UPPER-LEVEL CIRCUIT The UL circuitry is built around 1U2, a fast comparator that is similar to the LL comparator 1U3. The upper level is set by the front-panel potentiometer, 1R1, and is referenced to the -12-V NIM power supply. The setting on 1R1 is buffered by the unity gain stage 1U1(14). An inverting buffer, 1U1(8), connects the UL reference to the upper-level comparator at 1U2(4). When connected in the Integral or Normal mode, the input to the inverting buffer is from 1U1(14) and the UL reference voltage is fed to 1U2(4). When connected in the Window mode, the input to the inverting buffer is the sum of the LL reference, fed through 1R9, and the UL reference divided by 10, fed through 1R4. Thus, in the Window mode, the reference voltage at 1U2(4) is one-tenth the value of the UL setting plus the value of the LL setting. Offset voltages in the UL circuitry are corrected by the factory-set PWB potentiometer 1R36.

When the positive-going analog input signal causes 1U2(3) to become more positive than the reference level at 1U2(4), output 1U2(11) goes positive. This crossing of the upper, or window, level is latched in the set-reset flip-flop made up of the internal gate of 1U2 and gate 1U4(13). The second output at 1U2(9) connects to the input 1U2(4) through 1R24 to provide hysteresis to the upper-level comparator and prevent oscillations as the input signal crosses the upper-level reference voltage.

The positive-going signal at 1U2(11) triggers a negative-going one-shot signal at 1U8(4). This signal, nominally 500 ns wide, drives the hybrid output driver 1A3 which furnishes the UL Out signal on the rear panel.

SCA OUTPUT SIGNAL The signal at 1U5(6) determines if an SCA output signal will occur. The signal at 1U5(9) is positive or true if the lower-level crossing has been latched at 1U3(11). The signal at 1U5(10) is positive or true if the upper level or window crossing has not been latched at 1U2(11). Gate 1U5(12) provides the necessary inversion of the 1U2(11) signal as well as interfacing the setting of the 1W4 PWB jumpers which are associated

with the W4 jumper used to select Normal/Window or Integral mode. When the input signal recrosses the lower-level reference, 1U3(9) goes high. This trailing-edge crossing signal is inverted by 1U4(4) and 1U6(1) to produce 1U5(11) and cause an SCA output signal to occur.

The negative-going signal at 1U5(8) triggers a negative-going signal at 1U8(12) of 500 ns duration. This signal is inverted by the hybrid driver circuit 1A1 and provided at the SCA Out BNC connector on the front panel.

The signal at 1U5(8) also triggers a negative-going signal at 1U7(12) which drives a front-panel green Busy LED. The LED output is nominally 3 ms in duration and is updating.

RESET Reset begins when the input signal recrosses the lower-level reference setting. The signal 1U3(9) switches from low to high causing the signal at 1U4(4) to switch low and the signal at 1U4(10) to go high. However, 1U4 is an open-collector device, and the positive-going signal at 1U4(10) is controlled by the 1R35 and 1C23 time constant producing a fixed time delay. The actual reset signal is generated at 1U5(6) which will go low when all inputs to that gate are high. The signal at 1U5(5) is the latched, lower-level signal. The signal at 1U5(4) went high when the input signal recrossed the lower level, and the signal at 1U5(3) is the delayed signal. Reset is complete when both the lower-level and the upper-level latches are reset.

VOLTMETER The voltmeter section is shown on page 2 of the schematic. The voltmeter is built around U13, a 3-1/2 digit CMOS monolithic device. The voltage reference for U13 is D1, a bandgap reference diode. The input to the voltmeter is selected by the analog switch U15. Inputs "A" through "H" are from the unity gain buffer stages for the LL and UL of each channel. Selection of a given channel LL or UL is accomplished by the BCD signals at U15(9, 10, 11). Gates U18(3) and U18(6) form a set-reset flip-flop which drives counter U16(14). The counter outputs U16(9) and U16(12) select channel 1 through 4 at U15. Latch U19(6) is connected as a set-reset flip-flop. The output state at U19(9) toggles between the LL and the UL setting. U17 is a decoder that selects the front-panel LEDs associated with the voltmeter. U14 is an oscillator that is connected to the LED readout when the selected LL or UL voltage is adjusted beyond 9.99 V causing the display to flash at a nominal 2 Hz rate.

POWER Input power from the NIM bin and power supply is accepted through the module connector on the rear panel. The 850 operates on 145 mA from +12 V, 135 mA from -12 V, and 400 mA from +6 V. Power supply filtering and power distribution circuitry are shown on page 2 of the schematic. Q2 is used to drop the +6 V line to nominally +5 V to supply the majority of power for the logic circuits of the 850.

6. MAINTENANCE AND CALIBRATION

6.1. GENERAL

The basic performance of the 850 Quad Single-Channel Analyzer can be inferred from its operating responses. If the unit fails to respond properly at any time refer to Section 5 to determine the probable fault. The block diagram of Fig. 5.1 and schematic 687310 identify all of the circuits in the instrument.

6.2. FACTORY REPAIR

This instrument can be returned to EG&G ORTEC for service and repair at a nominal cost. Our standard procedure for repair ensures the same quality control and checkout that are used for a new instrument. Always contact the Customer Service Department at EG&G ORTEC, (615) 482-4411, before sending in an instrument for repair to obtain shipping instructions and so that the required Return Authorization Number can be assigned to the unit. Write this number on the address label and on the package to ensure prompt attention when it reaches the EG&G ORTEC factory.

6.3. TABULATED TEST POINT VOLTAGES

The voltages given in Table 6.1 are intended to indicate typical dc-levels that can be measured on the PWB. In some cases the circuit will perform satisfactorily even though, due to component tolerances, there may be some voltages that differ slightly from the listed values. Therefore, the tabulations should not be interpreted as absolute values but are intended to serve as an aid in troubleshooting. All voltages in Table 6.1 were measured with no input signal and with the mode jumpers set for Integral mode.

Table 6.1. Typical dc Voltages.

Location	Voltage
1R1-1R5 junction	-5
1R2-1R7 junction	-5
1U2(3)	0
1U2(11)	TTL-Low
1U2(13)	TTL-High
1U3(3)	0
1U3(9)	TTL-High
1U3(11)	TTL-Low
1U3(13)	TTL-High
1U4(10)	5
1U4(13)	TTL-Low
1U5(4)	TTL-High
1U5(6)	TTL-High
1U5(8)	TTL-High
Q2E	5
TP1-TP2	4.5
TP3-TP2	0.9

**BIN/MODULE CONNECTOR PIN ASSIGNMENTS
FOR STANDARD NUCLEAR INSTRUMENT
MODULES PER DOE/ER-0457T**

Pin	Function	Pin	Function
1	+3 volts	23	Reserved
2	-3 volts	24	Reserved
3	Spare Bus	25	Reserved
4	Reserved Bus	26	Spare
5	Coaxial	27	Spare
6	Coaxial	*28	+24 volts
7	Coaxial	*29	-24 volts
8	200 volts dc	30	Spare Bus
9	Spare	31	Spare
*10	+6 volts	32	Spare
*11	-6 volts	*33	117 volts ac (Hot)
12	Reserved Bus	*34	Power Return Ground
13	Spare	35	Reset (Scaler)
14	Spare	36	Gate
15	Reserved	37	Reset (Auxiliary)
*16	+12 volts	38	Coaxial
*17	-12 volts	39	Coaxial
18	Spare Bus	40	Coaxial
19	Reserved Bus	*41	117 volts ac (Neut.)
20	Spare	*42	High Quality Ground
21	Spare	G	Ground Guide Pin
22	Reserved		

Pins marked (*) are installed and wired in EG&G ORTEC's 4001A and 4001C Modular System Bins.